AN930.2: EFR32 Series 2 2.4 GHz Matching Guide

The EFR32 Series 2 devices include chip variants that provide 2.4 GHz-only operation. In addition, the EFR32xG21 chips are available in a 4x4 mm 32-pin QFN package. This application note describes the matching techniques applied to the EFR32 Series 2 Wireless Gecko Portfolio in the 2.4 GHz band.

For information on PCB layout requirements for proper 2.4 GHz operation, refer to AN928.2: EFR32 Series 2 Layout Design Guide.

KEY POINTS

- Description of the applied 2.4 GHz matching networks and techniques for the EFR32 Series 2 devices
- Detailed discussion of the design steps and design examples
- Measured TX fundamental and harmonic performance
- Noise figure for the whole RX chain

1. Device Compatibility

This application note supports the following devices:

EFR32 Series 2:

- EFR32 Mighty Gecko (EFR32MG21)
- EFR32 Blue Gecko (EFR32BG21)

2. Introduction

This application note is intended to help users achieve the best 2.4 GHz RF match for targeted applications. It describes the details of matching network design procedures and presents additional test results.

Thorough derivations of three different matching options are presented:

- 4-element discrete LC match for up to 0 dBm power levels
- 3-element PI discrete LC match for up to +10 dBm power levels
- 5-element PI discrete LC match for up to +20 dBm power levels

The 4x4 mm, 32-pin 2.4 GHz-only version's package pinout is shown in the figure below. The 2.4 GHz RF IO pins are highlighted with a red box.

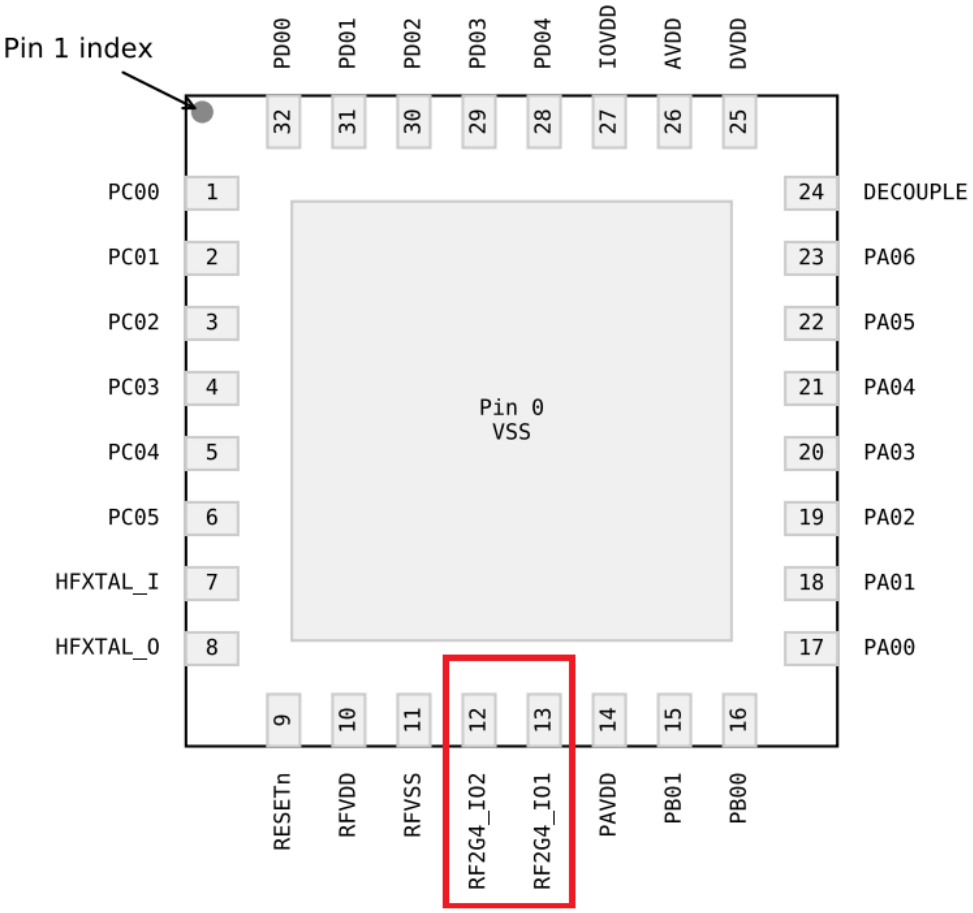


Figure 2.1. EFR32xG21 2.4 GHz RF IO Pins

2.1 Related Literature

Related documentation includes:

- AN928.2: EFR32 Series 2 Layout Design Guide
- AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations

3. EFR32xG21 RF Architecture Overview

The EFR32 Series 2 xG21 chip family has 2.4 GHz RF front ends only. The 2.4 GHz RF front end architecture is shown in the figure below. The 2.4 GHz antenna interface consists of two pins (RF2G4_IO1 and RF2G4_IO2) that interface directly to the on-chip BALUN.

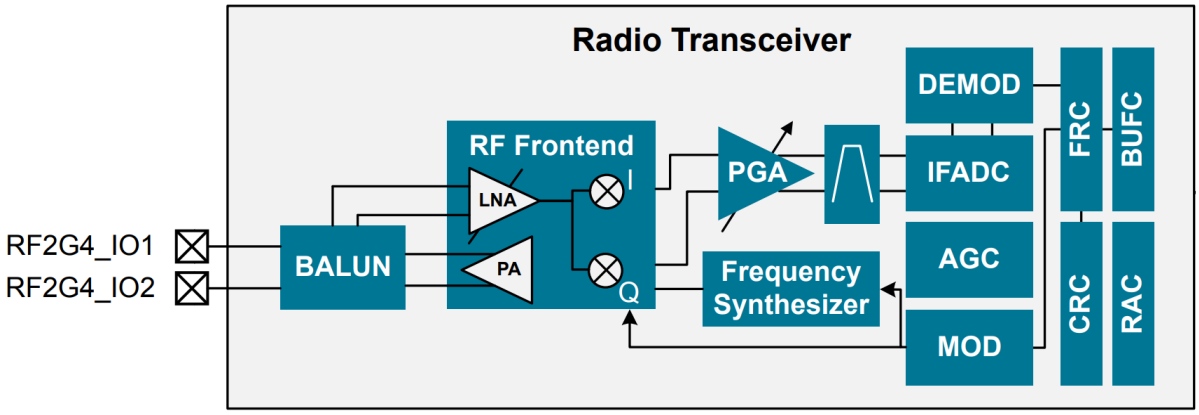


Figure 3.1. 2.4 GHz RF Front End Configuration

Several changes compared to the EFR32 Series 1 chip variants are highlighted below:

- New RF front-end topology: Three PAs included that require an optimal load impedance for each TX power level, i.e., different matches are required per max TX power.
- Power supply scheme: There is no on-chip DCDC converter available. Optimized for mains-power applications.
- Pre-Regulator for the Power Amplifiers: Linear regulator with an input of PAVDD and output of PA blocks. Regulates to a target voltage when PAVDD > Vtarget. Follows supply with a ~30 mV offset when PAVDD ≤ Vtarget (and PA power will trail off also).
  - For +10 and 0 dBm PA modes: Vtarget = 1.8 V.
  - For +20 dBm PA mode: Vtarget = 3.3 V.
- RFSENSE removed, instead a wide-band power sensing block introduced for better out-of-band blocker detection and coexistence performance.

The on-chip part of the front end comprises three PA structures optimized for the TX power levels of 0, 10, and 20 dBm, two differential LNAs, and an integrated balun. Each PA is biased through the PAVDD pin. Externally, a single-ended matching network and harmonic filtering are required.

- Differential Class-AB mode PA and an internal balun for TX power of +20 dBm
- Single-ended Class-D mode PA for TX power of +10 dBm
- Single-ended Class-D mode PA for TX power of 0 dBm
- Two LNAs
- Two RF IO ports available: Internal switches ground one of the two sides to create single-ended inputs / outputs on either RFIO pin. This also allows a switchless diversity solution, for instance.

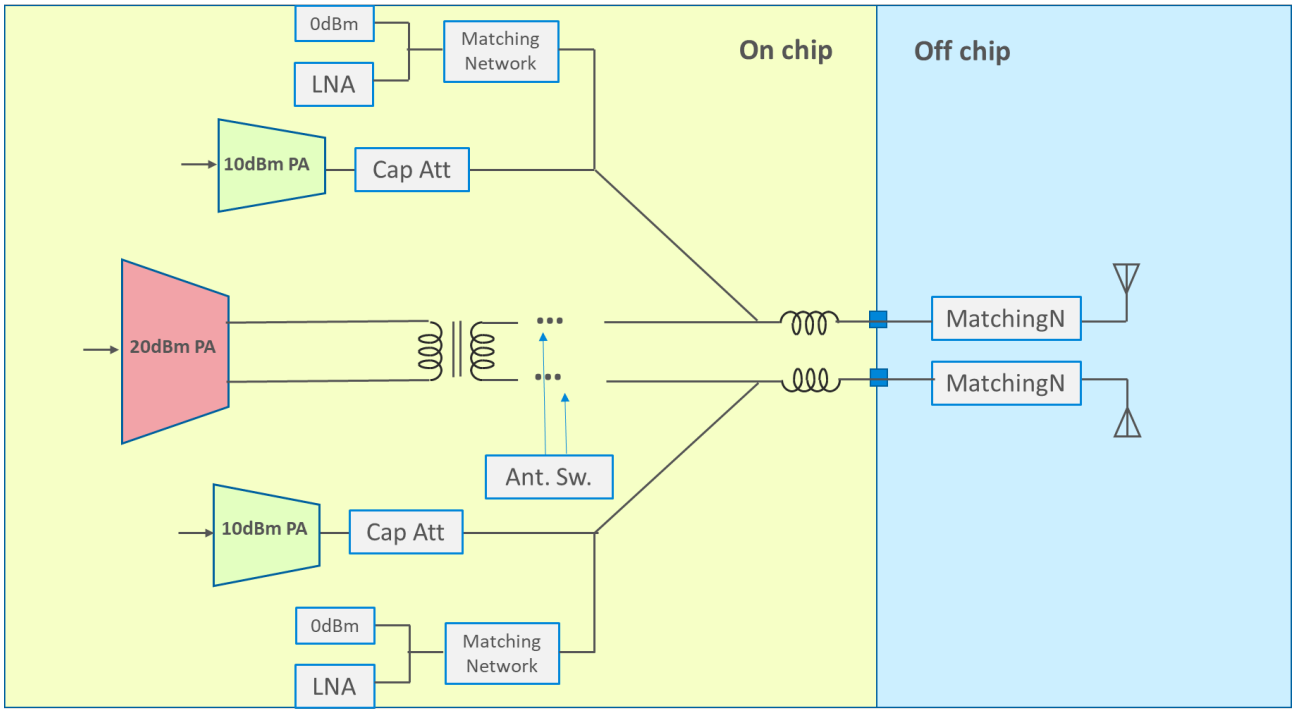


Figure 3.2. 2.4 GHz RF Front End Block Diagram

4. 2.4 GHz RF Matching Design Steps

2.4 GHz RF matching design for EFR32 chips consists of the following steps:

1. Determine the optimum termination impedance for the PA. Note that different matching topologies are recommended for different TX power levels as shown in the Introduction section.
2. Choose the RF matching topology.
3. Create the initial design with ideal, loss-free elements. This ideal design can be used as a starting point for a design with parasitics.
4. Design with parasitics and losses. At 2.4 GHz, the parasitics of the SMD elements and the pcb have a major effect, so tuning/optimization of the design is required. Here an optional EM simulation can be done, but simulations with well-estimated pcb parasitics and SMD equivalent models usually give adequate results.
5. Conduct bench testing and tuning.

4.1 Determining the Optimum Termination Impedance for the PA

The first step of the matching design procedure is to determine the optimum termination impedance at the PA. The realized matching network should present this impedance for the PA at the RF2G4_IO1/2 pin if 50 Ω termination is applied at the antenna port.

The RF2G4_IO1/2 RF port termination determines the major RF parameters, such as the delivered PA power and harmonic content in TX mode or the sensitivity in RX mode. As part of the design process, the goal is to deliver maximum power to a 50 Ω output termination (e.g., to a 50 Ω antenna) in TX mode. In addition, proper harmonic suppression and good RX sensitivity in reception mode are required.

The design target of optimum load impedance looking from the PA to the antenna is 14 + j5 at the PA. However, the optimum termination impedance for delivering maximum power in TX mode is determined by load-pull testing. The optimum termination impedance at the chip pin is determined for each PA of the EFR32xG21 parts and it slightly differs for the different power levels, i.e. for the +20, +10, and 0 dBm PAs, and also differs from the design target at the PA due to bonding wire inductances and parasitics. This termination impedance has to be shown by the matching network at the PA side if its antenna output is terminated with a 50 Ω load. The optimum termination impedance at chip RF2G4_IO pin is the following:

- For the **+20 dBm** PA: Zload_opt = **12 - j7 Ω**
- For the **+10 dBm** PA: Zload_opt = **17 - j5 Ω**
- For the **0 dBm** PA: Zload_opt = **17 + j3 Ω**

Applications with one antenna, e.g., non-diversity applications, typically require using only one of the RF IO ports available on the EFR32xG21 parts, in which case the recommended active RF IO port is **RF2G4_IO2**. Because this pin has a shorter on-chip, internal connection to the PA blocks so slightly lower parasitics appear on this pin.

The proper impedance at one of the single-ended RF2G4_IO pins also depends on the loading of the other RF2G4_IO pin. To keep its effect negligible, for applications with one antenna, it is recommended to directly tie the un-used RF2G4_IO pin back to the center GND pad of the chip. More detailed information about proper layout design can be found in application note, "AN928.2: EFR32 Series 2 Layout Design Guide".

In real radio links, the TX power and the receiver sensitivity together (i.e., the link budget) determine the range. So, with the applied TX termination impedance, the impedance match in RX mode should also be acceptable. Fortunately, the RX sensitivity is quite immune to impedance variations. The sensitivity variation is less than 0.5 dB if the termination changes from 50 Ω to the PA optimum impedance (Zload_opt) given above.

4.2 Choosing the RF Matching Topology

The second step of the matching design procedure is to choose the appropriate RF matching topology.

In addition to creating an optimum termination impedance on the IC side, the matching solution must exhibit sufficiently robust harmonic filtering characteristics to comply with emissions standards. There are many different types of RF matching topologies. Separate matching and harmonic filtering sections can be utilized, or they can be combined in one circuit. To minimize the number of elements, all matches presented here are of the combined type, with low-pass circuits employed for their inherent harmonic suppression characteristics.

Three 2.4 GHz matching topologies are presented here:

- 4-element discrete LC match for up to 0 dBm power levels, i.e., for the 0 dBm PA
- 3-element PI discrete LC match for up to +10 dBm power levels, i.e., for the +10 dBm PA
- 5-element PI discrete LC match for up to +20 dBm power levels, i.e., for the +20 dBm PA

4.3 Initial Design with Ideal, Loss-Free Elements

After choosing the appropriate topology for the application based on the TX power level requirements, the third step of the matching design procedure is to generate a lumped element schematic of the match with ideal loss-free elements and without PCB parasitics.

The matching circuit should show an input impedance of *Zload_opt* at the RF IO port of the chip while it is terminated by 50 Ω load at its output (ANT port). The impedance procedure is shown in the next sections, where, for simplification, the matching design is started from a termination impedance (*ZL*) which is the complex conjugate of the *Zload_opt* impedance. The reason is that the matching network will show the required *Zload_opt* impedance at its RF port only if it is perfectly matched there to a termination impedance which is the complex conjugate of the *Zload_opt* impedance.

The matching design process starts with a simplified case in which all losses and parasitics are eliminated. Here, parasitic-free ideal capacitors and inductors are used, and there are no PCB losses or parasitics. The real-world case can be derived later from this ideal design by means of incremental tuning and optimization.

4.4 Design with Parasitics and Losses

Silicon Labs reference designs utilize lumped elements in the RF matching network. At the operating frequency band of 2.4 GHz, the used SMD components and also the PCB parasitic effects need to be taken into account during the matching network design. The SMD components at these high-frequency ranges behave as a resonator. A capacitor can be realized by a series RLC resonant circuit, meanwhile an inductor's equivalent circuit represents a parallel RLC resonant circuit. Regarding the PCB parasitic effects, the series traces can be modeled as transmission lines with distributed L-C components, and can have considerable series parasitic inductance, while an SMD pad can behave as a parallel parasitic capacitance. For more details on the SMD parasitic descriptions and the rough estimation of PCB parasitics, refer to the application note, "AN930.1: EFR32 Series 1 2.4 GHz Matching Guide", and the SMD manufacturer website at www.murata.com, in regards to the appropriate SMD equivalent circuits.

The SMD components with different sizes have different parasitics, so it is also important to calculate with the appropriate values. Silicon Labs reference designs use **SMD 0201** components.

The recommended matching network for both RF ports is shown in the section Recommended Matching Networks. The circuit provides the optimum impedance load for the EFR32xG21 part while ensuring sufficient harmonic suppression. Some of the shunt capacitors are tuned to have self-resonances at the frequency ranges falling close to TX harmonics and therefore, they provide enhanced attenuation at specific harmonics. The impedance transformation procedure for each PA is shown in the Smith Chart figures below.

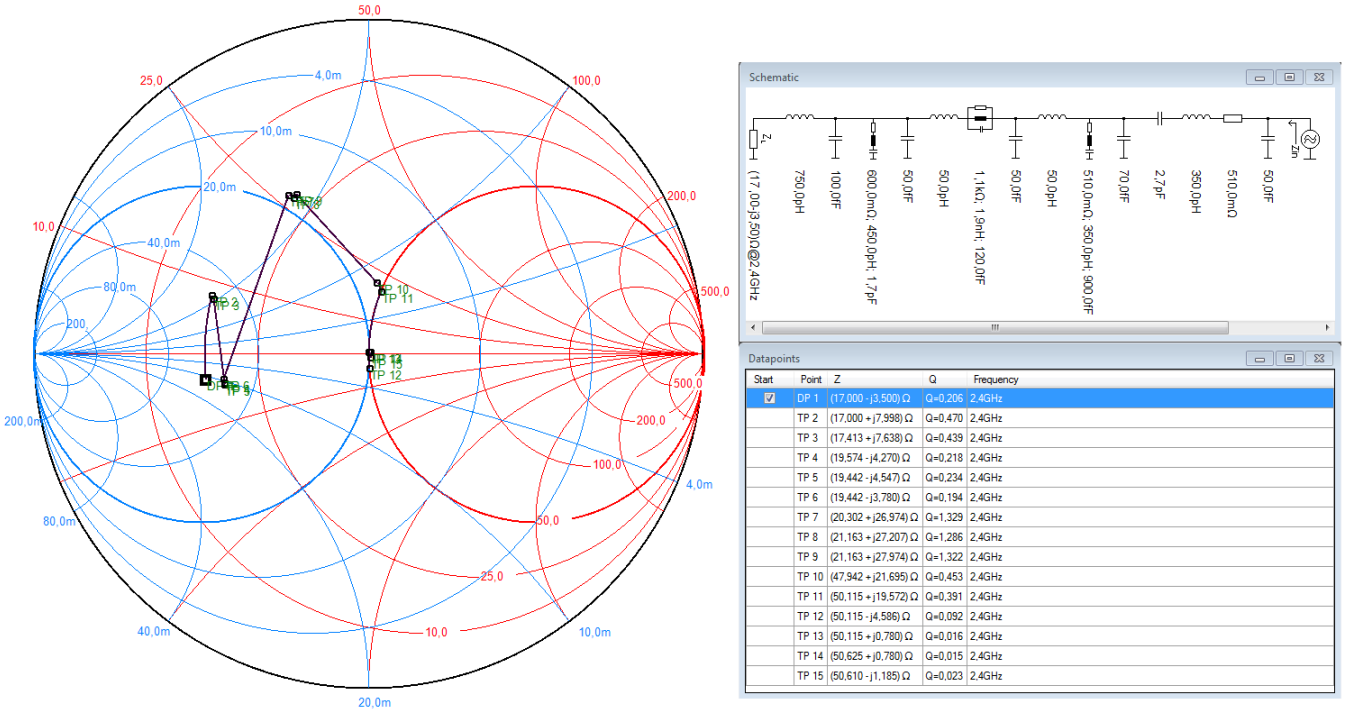


Figure 4.1. 4-element Match with SMD and PCB Layout Parasitics Tuned for the 0 dBm Power Level Optimum

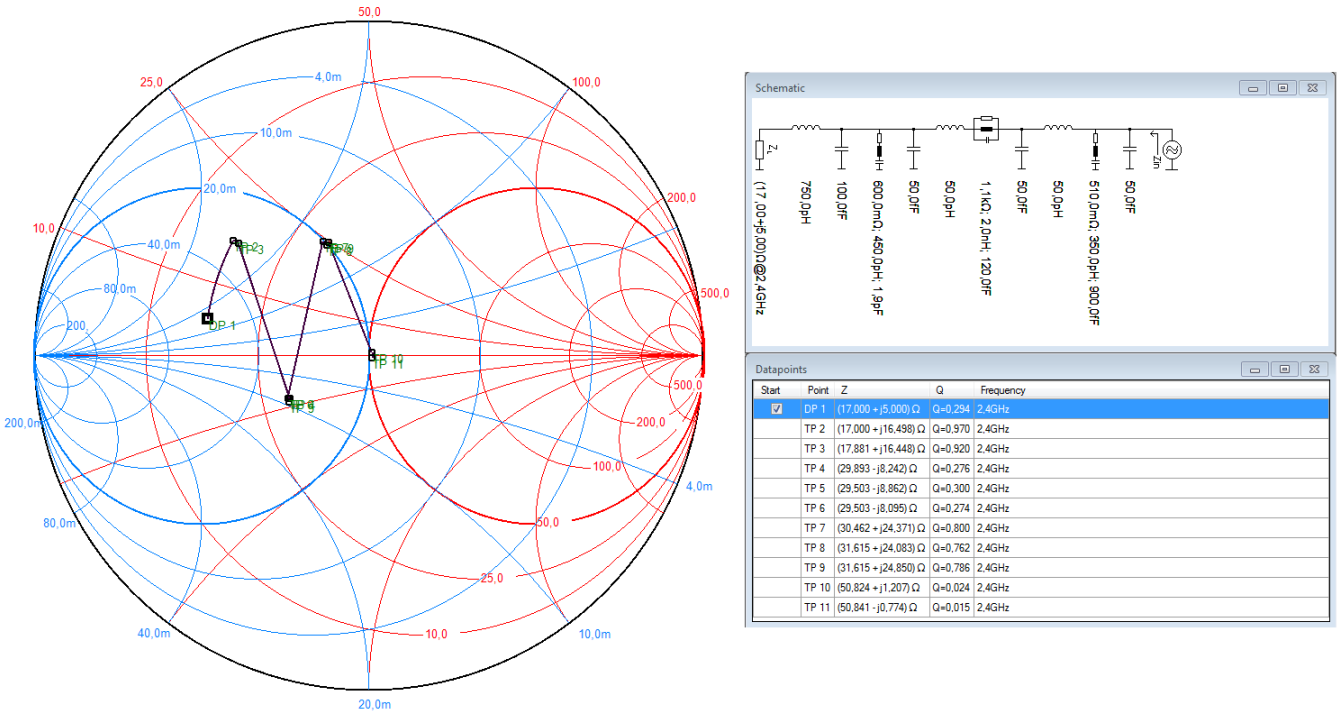


Figure 4.2. 3-element Match with SMD and PCB Layout Parasitics Tuned for the 10 dBm Power Level Optimum

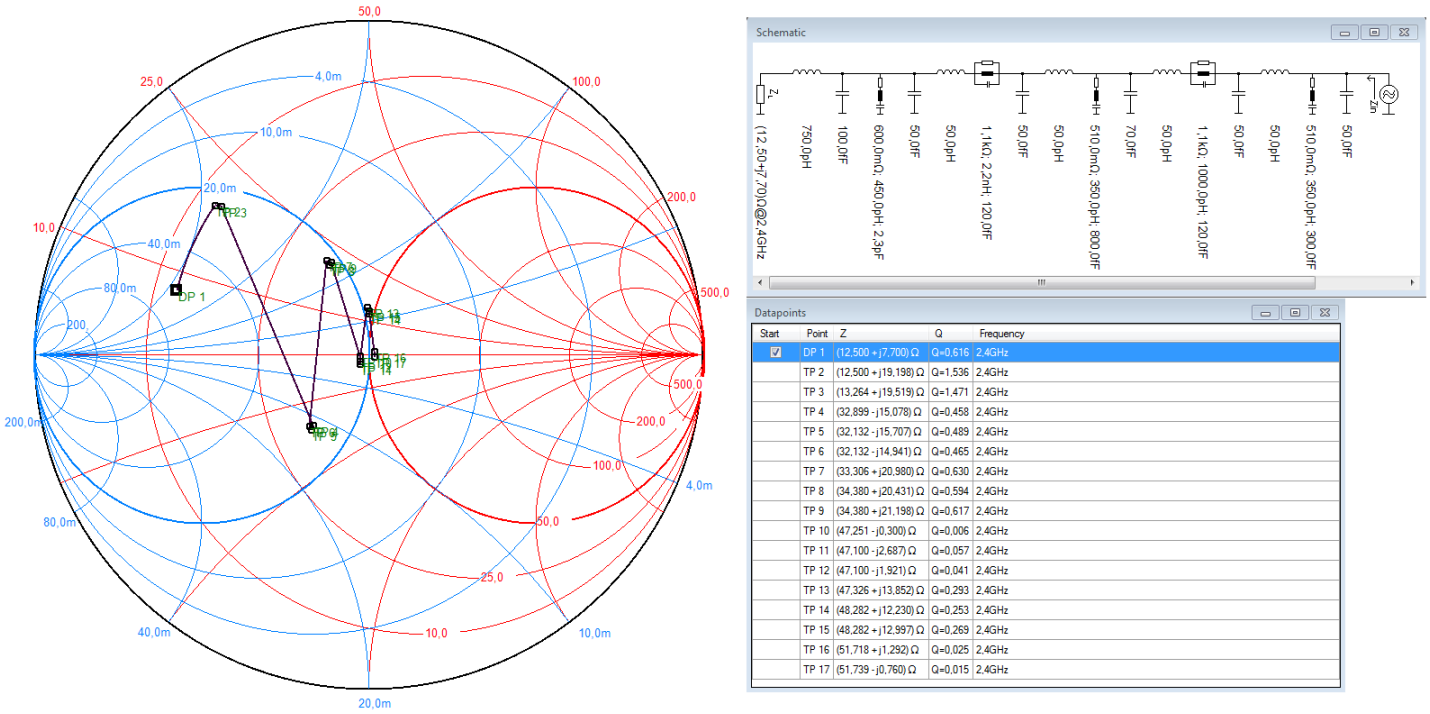


Figure 4.3. 5-element Match with SMD and PCB Layout Parasitics Tuned for the 20 dBm Power Level Optimum

4.5 Simulation Example on the 5-element Match for +20 dBm Power Level

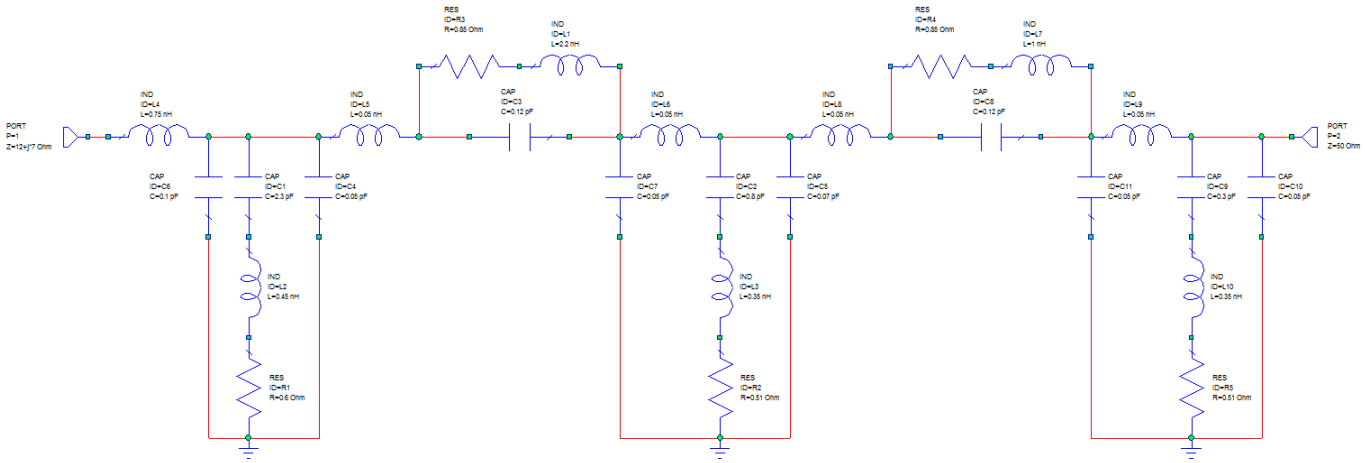


Figure 4.4. Discrete Schematic Model of 5-element Match with SMD and PCB Layout Parasitics

Port 1 (left-hand side-end) is the RF2G4_IO chip port/pin where the port impedance (*ZL*) should be set for the complex conjugate of optimum load impedance (*ZL=Zload_opt**), while the Port 2 (right end) is the 50-ohm antenna port.

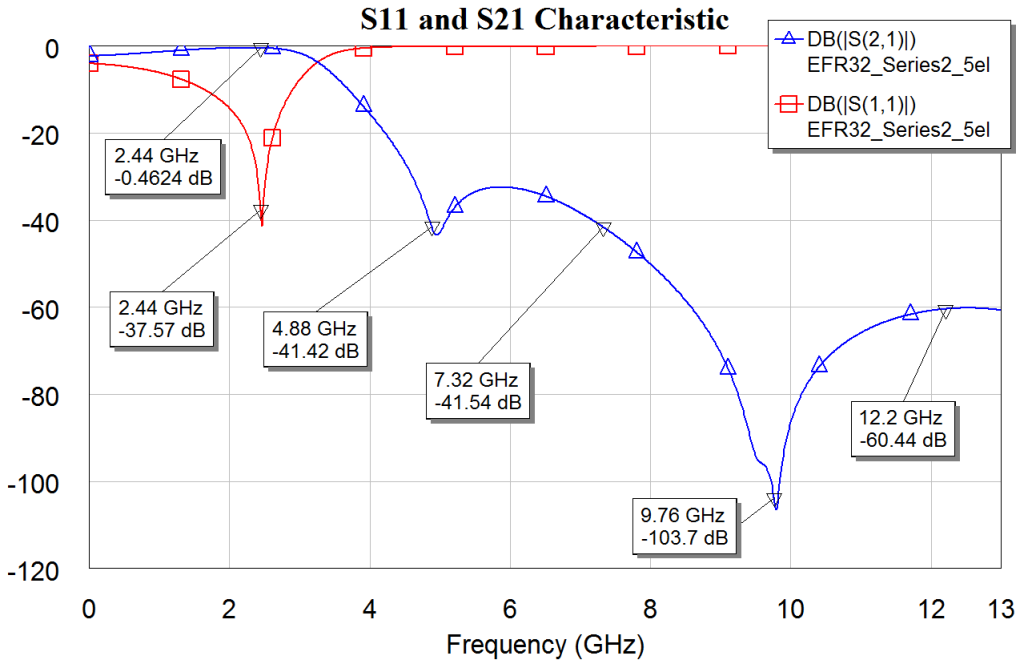


Figure 4.5. S11 and S21 Characteristics of 5-element Match for 20 dBm Power Level Optimum

5. Recommended Matching Networks

5.1 Recommended Matching Network for the 0 dBm PA

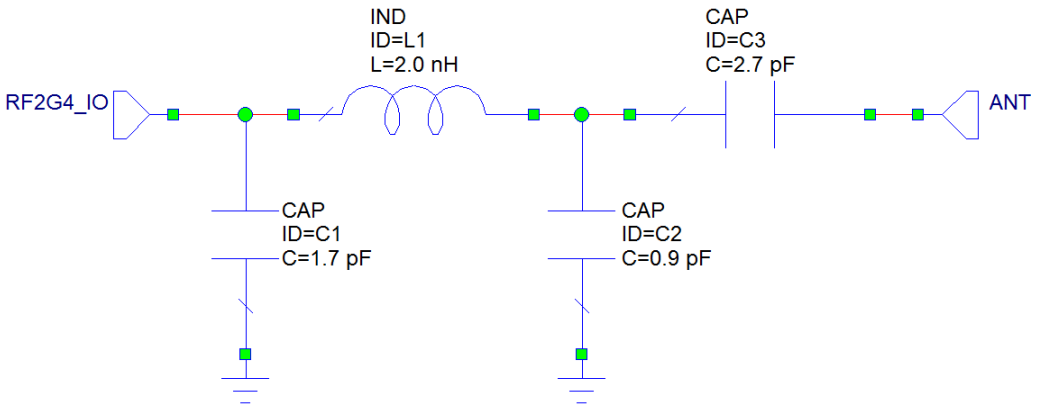


Figure 5.1. Matching Network Schematic for the 0 dBm PA

It is recommended to use this matching network shown above when the maximum transmitting power requirement is 0 dBm (TX power ≤ 0 dBm), i.e., the application utilizes the 0 dBm PA to achieve the possible best efficiency at that low power regions. Due to the highly optimized power efficiency, the need of 4-element matching network here is mostly driven by the harmonic suppression requirements.

Table 5.1. Final SMD Values for the 0 dBm PA (4-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.7 pF	± 0.5 %	GRM0335C1H1R7WA01D	Murata
L1	2.0 nH	± 0.1 nH	LQP03HQ2N0B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata
C3	2.7 pF	± 0.5 %	GRM0335C1H2R7WA01D	Murata

5.2 Recommended Matching Network for the +10 dBm PA

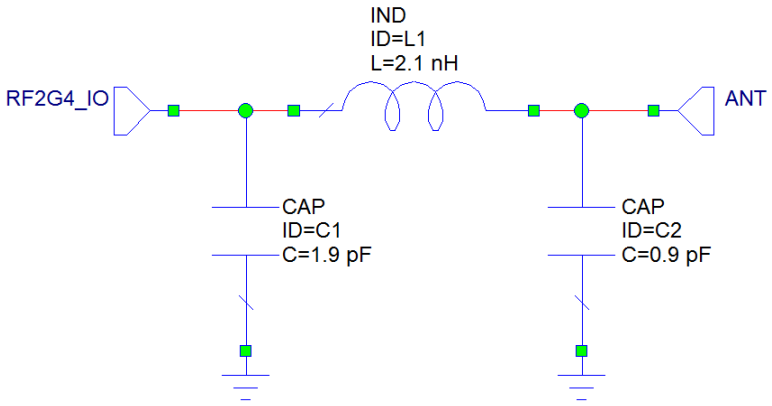


Figure 5.2. Matching Network Schematic for the +10 dBm PA

It is recommended to use the matching network shown above when the maximum transmitting power requirement is +10 dBm (0 dBm < TX power ≤ +10 dBm), i.e., the application utilizes the +10 dBm PA to achieve the possible best efficiency at that power level state.

Table 5.2. Final SMD Values for the +10 dBm PA (3-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	1.9 pF	± 0.5 %	GRM0335C1H1R9WA01D	Murata
L1	2.1 nH	± 0.1 nH	LQP03HQ2N1B02D	Murata
C2	0.9 pF	± 0.05 pF	GRM0335C1HR90WA01D	Murata

5.3 Recommended Matching Network for the +20 dBm PA

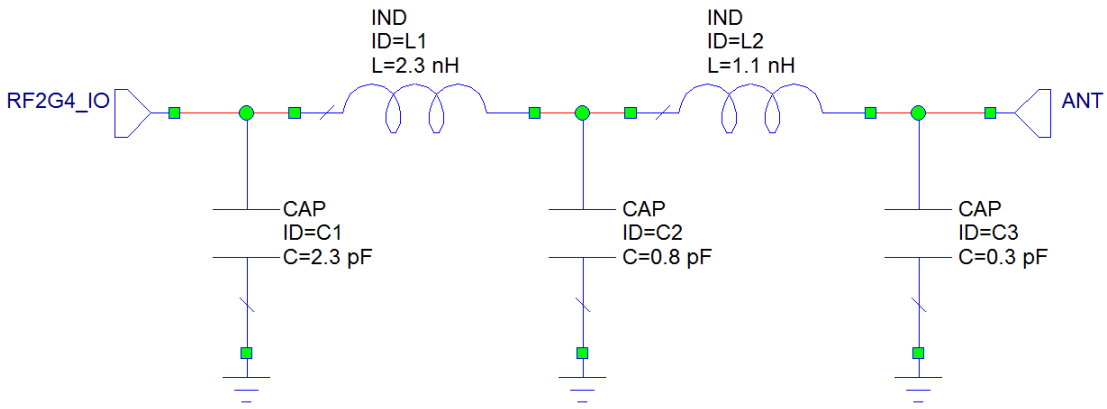


Figure 5.3. Matching Network Schematic for the +20 dBm PA

It is recommended to use the matching network shown above when the maximum transmitting power requirement is +20 dBm (+10 dBm < TX power ≤ +20 dBm), i.e., the application utilizes the +20 dBm PA to achieve the possible highest TX power level available. Due to the optimized power efficiency, the need for 5-element matching network here is mostly driven by the harmonic suppression requirements.

Table 5.3. Final SMD Values for the +20 dBm PA (5-element)

Schematic Reference Designator	Component Value	Tolerance	Part Number	Manufacturer
C1	2.3 pF	± 0.05 pF	GRM0335C1H2R3WA01D	Murata
L1	2.3 nH	± 0.1 nH	LQP03HQ2N3B02D	Murata
C2	0.8 pF	± 0.05 pF	GRM0335C1HR80WA01D	Murata
L2	1.1 nH	± 0.05 nH	LQP03HQ1N1W02D	Murata
C3	0.3 pF	± 0.05 pF	GRM0335C1HR30WA01D	Murata

5.4 Measurement Results

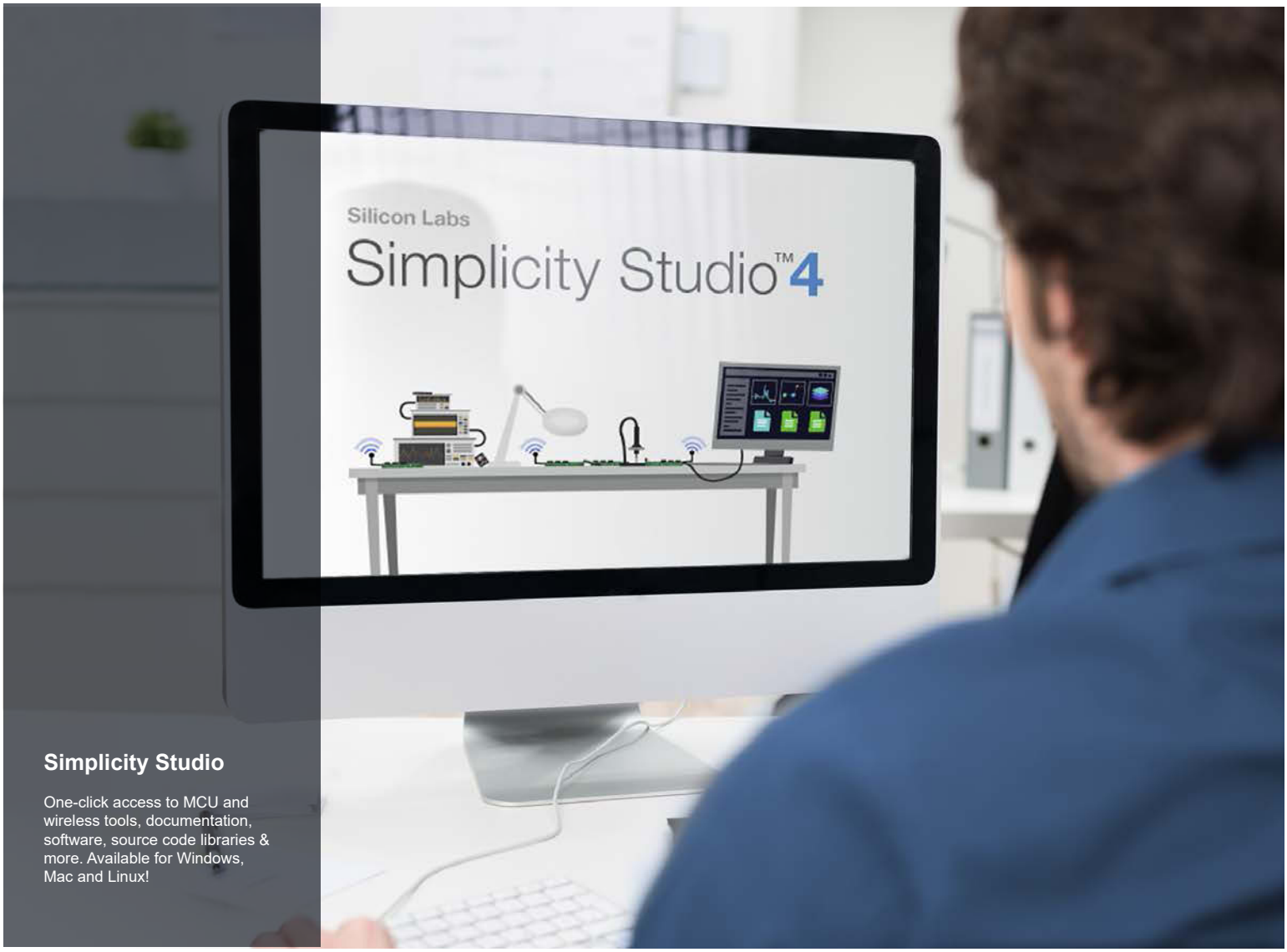
Table 5.4. Measurement Results for each Power Level (PA), Avg., Conducted

PA + Match used	NF [max.]	TX Power	PA current	H2 [max.]	H3 [max.]	H4 [max.]	H5 [max.]
0 dBm	7.1 dB	-0.5 dBm	4.3 mA	-60.1 dBm	-64.2 dBm	-67.9 dBm	-60.9 dBm
+10 dBm	7.0 dB	10.9 dBm	29.9 mA	-47.7 dBm	-48.8 dBm	-48.0 dBm	-48.0 dBm
+20 dBm	7.2 dB	20.2 dBm	178.1 mA	-55.4 dBm	-51.5 dBm	-52.1 dBm	-52.1 dBm

6. Revision History

February, 2019

Initial release.



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