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S720

SPI Configuration Guide

Issue 1.0

Notice

This document provides guide for users to use S720.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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About This Document

Scope

This document is applicable to the S720 series.

Audience

This document is intended for system engineers (SEs), development engineers, and test engineers.

Change History

Issue	Change	Changed By
1.0	Initial draft	Leo Shen

Conventions

Symbol	Indication
	Indicates danger or warning. This information must be followed. Otherwise, a catastrophic module or user device failure or bodily injury may occur.
	Indicates caution. This symbol alerts the user to important points about using the module. If these points are not followed, the module or user device may fail.
	Indicates instructions or tips. This symbol provides advices or suggestions that may be useful when using the module.

1 Overview

Serial Peripheral Interface (SPI) is a synchronous serial interface technology introduced by Motorola. It is a high-speed, full-duplex, synchronous communication bus.

The S720 platform provides two SPIs that can be used by customers as desired: SPI0 and SPI1.

SPI ID	Function description	Pin	GPIO ID	Remarks	Function (default)
spi0	SPI0_CSN	pin-117	GPIO-90	Chip Select	Other function
	SPI0_DO	pin-119	GPIO-91	Host TX	Other function
	SPI0_DI	pin-118	GPIO-92	Host RX	Other function
	SPI0_CLK	pin-116	GPIO-93	Clock	Other function
spi2	SPI2_CSN	pin-107	GPIO-52	Chip Select	Other function
	SPI2_DO	pin-108	GPIO-53	Host TX	Other function
	SPI2_DI	pin-109	GPIO-54	Host RX	Other function
	SPI2_CLK	pin-110	GPIO-55	Clock	Other function

The SPI pin functions are configured in the pinmap of uboot, and the SPI node and device node are configured in the DTS of the Kernel. For the specific configuration method, see the following context.

2 Pinmap Configuration

S720 uses the pinmap to configure the pin function. To use the SPI function, you need to check the table below and configure the SPI function for the corresponding pin.

Open the pinmap file, **pinmap-sl8541e.c**, in the **bsp\bootloader\u-boot15\board\spreadtrum\S720** directory.

Cell Name	Pin Name	Function0	Type	Function1	Type	Function2	Type	Function3	Type
SPSCBC2_8X_VL	SPI0_CSN	SPI0_CSN	I/O/T			EXTINT5	I	GPIO90	I/O/T
SPSCBC2_8X_VL	SPI0_DO	SPI0_DO	I/O/T			EXTINT6	I	GPIO91	I/O/T
SPSCBC2_8X_VL	SPI0_DI	SPI0_DI	I/O/T			EXTINT7	I	GPIO92	I/O/T
SPSCBC2_8X_VL	SPI0_CLK	SPI0_CLK	I/O/T			EXTINT8	I	GPIO93	I/O/T
SPSCBC2_8X_VL	SPI2_CSN	SPI2_CSN	I/O/T			CM4_GPIO5	I/O/T	GPIO52	I/O/T
SPSCBC2_8X_VL	SPI2_DO	SPI2_DO	I/O/T			CM4_GPIO0	I/O/T	GPIO53	I/O/T
SPSCBC2_8X_VL	SPI2_DI	SPI2_DI	I/O/T			CM4_GPIO1	I/O/T	GPIO54	I/O/T
SPSCBC2_8X_VL	SPI2_CLK	SPI2_CLK	I/O/T			CM4_GPIO2	I/O/T	GPIO55	I/O/T

For example, to configure SPI0, modify the pinmap as follows:

```
// spi0, cs
{REG_PIN_SPI0_CSN,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CSN,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPU|BIT_PIN_SLP_AP|BIT_PIN_SLP_NUL|BIT_PIN_SLP_OE},
// spi0, DO
{REG_PIN_SPI0_DO,       BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DO,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0, DI
{REG_PIN_SPI0_DI,       BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DI,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0, CLK
{REG_PIN_SPI0_CLK,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CLK,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
```

3 DTS Configuration

3.1 Confirming the Aliases Node

Add the configuration of the SPI node (for example, SPI0) under the aliases node.

Open **S720_sharkle.dtsi** in the **bsp\kernel\kernel4.14\arch\arm\boot\dts** directory. Then confirm the following code.

```
    aliases {
       ...
  spi0 = &spi0;
...
    };
```

3.2 Confirming the SPI Node

Add the configuration of the SPI.

For example, SPI0 under the SOC node. Open **S720_sharkle.dtsi** in the **bsp\kernel\kernel4.14\arch\arm\boot\dts** directory. Then confirm the following code.

```
    spi0: spi@70a00000 {
        compatible = "sprd,sc9860-spi",
            "sprd,sharkle-spi";
        reg = <0x70a00000 0x1000>;  /*spi0 register address*/
        interrupts = <GIC_SPI 7 IRQ_TYPE_LEVEL_HIGH>; /*interrupt number*/
        #address-cells = <1>;
        #size-cells = <0>;
        status = "disabled"; /*Before using, please enable the node: okay*/
    };
```

Generally, the I2C node is already configured, and you only need to check and confirm the configuration.

3.3 Adding an SPI Device Node

After configuring the SPI node, add the corresponding SPI device node.

For example, FPGA node. Open **S720_sl8541e.dtsi** in the **bsp\kernel\kernel4.14\arch\arm\boot\dts** directory. Then configure the following code:

```
&spi0 {
    status = "okay"; /*enable spi: okay*/
    fpga: fpga {
        compatible = "lattice-spi";
        spi-max-frequency = <48000000>; /*spi clock frequency*/
        crstn-gpio = <&ap_gpio 133 0>;
        rstn-gpio = <&ap_gpio 132 0>;
        reg = <0>;
    };
};
```


4 Configuration of SPIs

4.1 Configuring SPI-0

Step 1: Configure the pinmap. Check the function table, which shows that function 0 is the SPI-0 function.

Open **pinmap-sl8541e.c** in the **bsp\bootloader\u-boot15\board\spreadtrum\S720** directory. Then configure the following code:

```
// spi0 cs
{REG_PIN_SPI0_CSN,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CSN,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPU|BIT_PIN_SLP_AP|BIT_PIN_SLP_NUL|BIT_PIN_SLP_OE},
// spi0 DO
{REG_PIN_SPI0_DO,       BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DO,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0 DI
{REG_PIN_SPI0_DI,       BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DI,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0 CLK
{REG_PIN_SPI0_CLK,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CLK,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
```

Step 2: Confirm the aliases node.

Open **S720_sharkle.dtsi** in the **bsp\kernel\kernel4.14\arch\arm\boot\dts** directory. Then confirm the following code:

```
    aliases {
...
        spi0 = &spi0;
...
    };
    spi0: spi@70a00000 {
        compatible = "sprd,sc9860-spi",
            "sprd,sharkle-spi";
        reg = <0x70a00000 0x1000>;
        interrupts = <GIC_SPI 7 IRQ_TYPE_LEVEL_HIGH>;
        #address-cells = <1>;
        #size-cells = <0>;
        status = "disabled";
    };
```

4.2 Configuring SPI-2

Step 1: Configure the pinmap. Check the function table, which shows that function 0 is the SPI-2 function.

Open **pinmap-sl8541e.c** in the **bsp\bootloader\u-boot15\board\spreadtrum\S720** directory. Then configure the following code:

```
// spi2, CSN
{REG_PIN_SPI2_CSN,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI2_CSN,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPU|BIT_PIN_SLP_AP|BIT_PIN_SLP_NUL|BIT_PIN_SLP_OE},
// spi2, DO
{REG_PIN_SPI2_DO,       BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI2_DO,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi2, DI
{REG_PIN_SPI2_DI,       BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI2_DI,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi2, CLK
{REG_PIN_SPI2_CLK,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI2_CLK,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
```

Step 2: Confirm the aliases node.

Open **S720_sharkle.dtsi** in the **bsp\kernel\kernel4.14\arch\arm\boot\dts** directory. Then confirm the following code:

```
    aliases {
...
        spi2 = &spi2;
...
    };
```

```
    spi2: spi@70c00000 {
        compatible = "sprd,sc9860-spi",
            "sprd,sharkle-spi";
        reg = <0x70c00000 0x1000>;
        interrupts = <GIC_SPI 9 IRQ_TYPE_LEVEL_HIGH>;
        #address-cells = <1>;
        #size-cells = <0>;
        status = "disabled";
    };
```