

S726

SPI Configuration Guide

Issue 1.0



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Notice

This document provides guide for users to use S726.

This document is intended for system engineers (SEs), development engineers, and test engineers.

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About This Document

Scope

This document is applicable to the S726 series.




Audience

This document is intended for [system engineers \(SEs\)](#), [development engineers](#), and [test engineers](#).

Change History

Issue	Change	Changed By
1.0	Initial draft	Leo Shen

Conventions

Symbol	Indication
	Indicates danger or warning. This information must be followed. Otherwise, a catastrophic module or user device failure or bodily injury may occur.
	Indicates caution. This symbol alerts the user to important points about using the module. If these points are not followed, the module or user device may fail.
	Indicates instructions or tips. This symbol provides advices or suggestions that may be useful when using the module.

1 Overview

Serial Peripheral Interface (SPI) is a synchronous serial interface technology introduced by Motorola. It is a high-speed, full-duplex, synchronous communication bus.

The S726 platform provides two SPIs that can be used by customers as desired: SPI0 and SPI1.

SPI ID	Function description	Pin	GPIO ID	Remarks	Function (default)
spi0	SPI0_DO	pin-112	GPIO-91	Host TX	GPIO function
	SPI0_DI	pin-113	GPIO-92	Host RX	GPIO function
	SPI0_CSN	pin-123	GPIO-90	Chip Select	GPIO function
	SPI0_CLK	pin-124	GPIO-93	Clock	GPIO function
spi1	SPI1_DO	pin-119	GPIO-136	Host TX	SDIO interface
	SPI1_DI	pin-118	GPIO-135	Host RX	SDIO interface
	SPI1_CSN	pin-117	GPIO-139	Chip Select	SDIO interface
	SPI1_CLK	pin-116	GPIO-134	Clock	SDIO interface

The SPI pin functions are configured in the pinmap of uboot, and the SPI node and device node are configured in the DTS of the Kernel. For the specific configuration method, see the following steps.

2 Pinmap Configuration

S726 uses the pinmap to configure the pin function. To use the SPI function, you need to check the table below and configure the SPI function for the corresponding pin.

Open the pinmap file, **pinmap-sp9863a.c**, in the **bsp\bootloader\u-boot15\board\spreadtrum\S726** directory.

Cell Name	Pin Name	Function0	Type	Function1	Type	Function2	Type	Function3	Type
SPSCBC2_8X_IC_HL	SCL2	SCL2	I/O/T					GPIO127	I/O/T
SPSCBC2_8X_IC_HL	SDA2	SDA2	I/O/T					GPIO128	I/O/T
SPSCBC2_8X_W_IC_HL	SCL3	SCL3	I/O/T			EXT_XTL_EN0	I	GPIO146	I/O/T
SPSCBC2_8X_W_IC_HL	SDA3	SDA3	I/O/T					GPIO147	I/O/T
SPPDWUWSW_SIM_V	SIMCLK2	SIMCLK2	O	SCL4	I/O/T	SE_GPIO1_1	I/O/T	GPIO154	I/O/T
SPPDWUWSW_SIM_V	SIMDAT2	SIMDAT2	I/O/T	SDA4	I/O/T	SE_GPIO1_2	I/O/T	GPIO155	I/O/T
SPSCBC2_8X_IC_HL	U5TXD	U5TXD	O	SCL5	I/O/T			GPIO38	I/O/T
SPSCBC2_8X_IC_HL	U5RXD	U5RXD	I	SDA5	I/O/T			GPIO39	I/O/T

For example, to configure SPI0, modify the pinmap as follows:

```
// spi0, cs
{REG_PIN_SPI0_CSN,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CSN,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPU|BIT_PIN_SLP_AP|BIT_PIN_SLP_NUL|BIT_PIN_SLP_OE},
// spi0, DO
{REG_PIN_SPI0_DO,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DO,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0, DI
{REG_PIN_SPI0_DI,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DI,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0, CLK
{REG_PIN_SPI0_CLK,     BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CLK,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
```

3 DTS Configuration

3.1 Confirming the aliases Node

Add the configuration of the SPI node (for example, SPI0) under the aliases node.

Open **sharkl3.dtsi** in the **bsp\kernel\kernel4.14\arch\arm64\boot\dts\sprd** directory. Then confirm the following code.

```
aliases {
    ...
    spi0 = &spi0;
    ...
};
```

3.2 Confirming the SPI Node

Add the configuration of the SPI.

For example, SPI0 under the SOC node. Open **sharkl3.dtsi** in the **bsp\kernel\kernel4.14\arch\arm64\boot\dts\sprd** directory. Then confirm the following code.

```
spi0: spi@70a00000{
    compatible = "sprd,sc9863-spi";
    reg = <0x70a00000 0x1000>; /*spi0 register address*/
    interrupts = <GIC_SPI 7 IRQ_TYPE_LEVEL_HIGH>; /*interrupt number*/
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled"; /*before using, please enable the node: okay*/
};
```

Generally, the I2C node is already configured, and you only need to check and confirm the configuration.

3.3 Adding an SPI Device Node

After configuring the SPI node, add the corresponding SPI device node.

For example, FPGA node. Open **S726_uis8581e5h10.dts** in the **bsp\kernel\kernel4.14\arch\arm64\boot\dts\sprd** directory. Then configure the following code:

```
&spi0 {
    status = "okay"; /*enable spi: okay*/
```

```
fpga: fpga {
    compatible = "lattice-spi";
    spi-max-frequency = <48000000>; /*spi clock frequency*/
    crstn-gpio = <&ap_gpio 133 0>;
    rstn-gpio = <&ap_gpio 132 0>;
    reg = <0>;
};
};
```


4 Configuration of SPIs

4.1 Configuring SPI-0

Step 1: Configure the pinmap. Check the function table, which shows that function 0 is the SPI-0 function.

Open **S726\pinmap-sp9863a.c** in the **bsp\bootloader\u-boot15\board\spreadtrum** directory. Then configure the following code:

```
// spi0 cs
{REG_PIN_SPI0_CSN,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CSN,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPU|BIT_PIN_SLP_AP|BIT_PIN_SLP_NUL|BIT_PIN_SLP_OE},
// spi0 DO
{REG_PIN_SPI0_DO,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DO,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0 DI
{REG_PIN_SPI0_DI,      BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_DI,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi0 CLK
{REG_PIN_SPI0_CLK,     BITS_PIN_AF(0)},
{REG_MISC_PIN_SPI0_CLK,
BITS_PIN_DS(1)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
```

Step 2: Confirm the aliases node.

Open **sharkl3.dtsi** in the **bsp\kernel\kernel4.14\arch\arm64\boot\dts\sprd** directory. Then confirm the following code:

```
aliases {
...
    spi0 = &spi0;
...
};
spi0: spi@70a00000{
    compatible = "sprd,sc9863-spi";
    reg = <0x70a00000 0x1000>;
    interrupts = <GIC_SPI 7 IRQ_TYPE_LEVEL_HIGH>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```

4.2 Configuring SPI-1

Step 1: Configure the pinmap. Check the function table, which shows that function 1 is the SPI-1 function.

Open **sharkl3.dtsi** in the **bsp/kernel/kernel4.14/arch/arm64/boot/dts/sprd** directory. Then configure the following code:

```
// spi1, clk
{REG_PIN_SD2_CLK,    BITS_PIN_AF(1)},
{REG_MISC_PIN_SD2_CLK,
BITS_PIN_DS(3)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi1, DO
{REG_PIN_SD2_D0,    BITS_PIN_AF(1)},
{REG_MISC_PIN_SD2_D0,
BITS_PIN_DS(3)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi1, DI
{REG_PIN_SD2_CMD,    BITS_PIN_AF(1)},
{REG_MISC_PIN_SD2_CMD,
BITS_PIN_DS(3)|BIT_PIN_NULL|BIT_PIN_WPD|BIT_PIN_SLP_AP|BIT_PIN_SLP_WPD|BIT_PIN_SLP_Z},
// spi1, CSN
{REG_PIN_SD2_D3,    BITS_PIN_AF(1)},
{REG_MISC_PIN_SD2_D3,
BITS_PIN_DS(3)|BIT_PIN_NULL|BIT_PIN_WPU|BIT_PIN_SLP_AP|BIT_PIN_SLP_NUL|BIT_PIN_SLP_OE},
```

Step 2: Confirm the aliases node.

Open **sharkl3.dtsi** in the **bsp/kernel/kernel4.14/arch/arm64/boot/dts/sprd** directory. Then confirm the following code:

```
aliases {
...
    spi1 = &spi1;
...
};
```

```
spi1: spi@70b00000{
    compatible = "sprd,sc9863-spi";
    reg = <0x70b00000 0x1000>;
    interrupts = <GIC_SPI 8 IRQ_TYPE_LEVEL_HIGH>;
    #address-cells = <1>;
    #size-cells = <0>;
    status = "disabled";
};
```