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1. Electrical Characteristics

V_{DD}= 3.3 V, T_{OP}= 25 °C, F_{RF} = 433.92 MHz, the sensitivity is measured by receiving a PN9 coded data and matching the impedance to 50Ωunder the 0.1%BER standard.Unless otherwise stated, all results are tested on theCMT2218B-EM evaluation board.

1.1 Recommended OperationCondition

Table 1. Recommended operation condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
Power voltage slope			1			mV/us

1.2 Absolute Maximum Rating

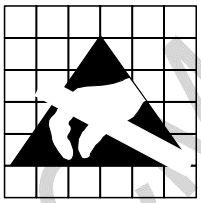
Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} +0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating[2]		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Notes:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2].



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Table 3. Power consumption specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleepcurrent	I_{SLEEP}	Sleep mode, sleep timeris off		300		nA
		Sleep mode, sleep timeris on		800		nA
RXcurrent(high powermode)	I_{Rx-HP}	FSK, 433 MHz, 10 kbps,10 kHz F_{DEV}		8.5		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		8.6		mA
		FSK, 915 MHz, 10 kbps,10 kHz F_{DEV}		8.9		mA
RXcurrent(low power mode)	I_{Rx-LP}	FSK, 433 MHz, 10 kbps, 10 kHz F_{DEV}		7.2		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		7.3		mA
		FSK, 915 MHz, 10 kbps, 10 kHz F_{DEV}		7.6		mA

1.4 Receiver

Table 4. Receiver specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR	OOK	0.5		40	kbps
		FSK and GFSK	0.5		300	kbps
Deviation	F_{DEV}	FSK and GFSK	2		200	kHz
Sensitivity @ 433 MHz	S_{433-HP}	DR = 2.0 kbps, F_{DEV} = 10 kHz		-121		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-116		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low powersetting）		-115		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power setting）		-112		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-111		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-108		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-105		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--103		dBm
Sensitivity @ 868 MHz	S_{868-HP}	DR = 2.0 kbps, F_{DEV} = 10 kHz		-119		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low powersetting）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power setting）		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-108		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Sensitivity @ 915 MHz	S_{915-HP}	DR = 2.0 kbps, F_{DEV} = 10 kHz		-117		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power mode）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power mode）		-109		dBm

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--99		dBm
Saturation Input Signal Level	P_{LVL}				20	dBm
Image Rejection Ratio	IMR	F_{RF}=433 MHz		35		dBc
		F_{RF}=868 MHz		33		dBc
		F_{RF}=915 MHz		33		dBc
RX Channel Bandwidth	BW	RX channel bandwidth	50		500	kHz
Co-channel Rejection Ratio	CCR	DR = 10 kbps, F_{DEV} = 10 kHz; Interference with the same modulation		-7		dBc
Adjacent Channel Rejection Ratio	ACR-I	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 200 kHzChannel spacing, interference with the same modulation		30		dBc
AlternateChannel Rejection Ratio	ACR-II	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100kHz, 400 kHzChannel spacing, interference with the same modulation		45		dBc
Blocking Rejection Ratio	BI	DR = 10 kbps, F_{DEV} = 10 kHz; ±1 MHzDeviation, continuous wave interference		70		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ± 2 MHzDeviation, continuous wave interference		72		dBc
		DR = 10 kbps, F_{DEV} = 10 kHz; ±10 MHzDeviation, continuous wave interference		75		dBc
Input 3rd Order Intercept Point	IIP3	DR = 10 kbps, F_{DEV} = 10 kHz; 1 MHz and 2 MHz Deviation dual tone test, maximum system gain setting.		-25		dBm
RSSIRange	RSSI		-120		20	dBm
More Sensitivity (Typical Configuration)		433.92 MHz, DR = 1.2kbps, F_{DEV} = 5 kHz		-122.9		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 10 kHz		-121.8		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 20 kHz		-119.5		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 5 kHz		-120.6		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 10 kHz		-120.3		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 20 kHz		-119.7		dBm
		433.92 MHz, DR = 9.6 kbps, F_{DEV} = 9.6 kHz		-116.0		dBm
		433.92 MHz, DR = 9.6 kbps, FDEV = 19.2 kHz		-116.1		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 10 kHz		-114.2		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 20 kHz		-113.0		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 25 kHz		-110.6		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 50 kHz		-109.0		dBm
		433.92 MHz, DR = 100 kbps, FDEV = 50 kHz		-107.8		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 50 kHz		-103.5		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 100 kHz		-104.3		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 50 kHz		-98.0		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 150 kHz		-101.6		dBm

1.5 SettleTime

Table 5. SettleTime

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settle time	T_{SLP-RX}	From Sleep to RX		1000		us
Note: [1]. $T_{SLP-RX}$is dominated by the crystal oscillator startup time, which depends on its own characteristics.						

1.6 Frequency Synthesizer

Table 6. Frequency Synthesizer Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Need different matching networks	760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase noise@ 433 MHz	PN_{433}	10 kHz frequency deviation		-94		dBc/Hz
		100 kHz frequency deviation		-99		dBc/Hz
		500 kHz frequency deviation		-118		dBc/Hz
		1MHz frequency deviation		-127		dBc/Hz
		10 MHz frequency deviation		-134		dBc/Hz
Phase noise@ 868 MHz	PN_{868}	10 kHz frequency deviation		-92		dBc/Hz
		100 kHz frequency deviation		95		dBc/Hz
		500 kHz frequency deviation		-114		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz
Phase noise@ 915 MHz	PN_{915}	10 kHz frequency deviation		-89		dBc/Hz
		100 kHz frequency deviation		-92		dBc/Hz
		500 kHz frequency deviation		-111		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz

1.7 Crystal Oscillator

Table 7. Crystal Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Equivalent resistance	Rm			60		Ω
Start-up time[3]	t_{XTAL}			400		us
Remarks:						

[1]. CMT2218B can use the external reference clock to drive the XIN pin through the coupling capacitor. The peak value of the external clock signal is between 0.3V and 0.7V.
[2]. The value includes (1) initial error; (2) crystal load; (3) aging; and (4) change with temperature. The acceptable crystal frequency tolerance is limited by the receiver bandwidth and the RF frequency offset between the transmitter and the receiver.
[3]. The parameter is largely related to the crystal.

1.8 Low Frequency Oscillator

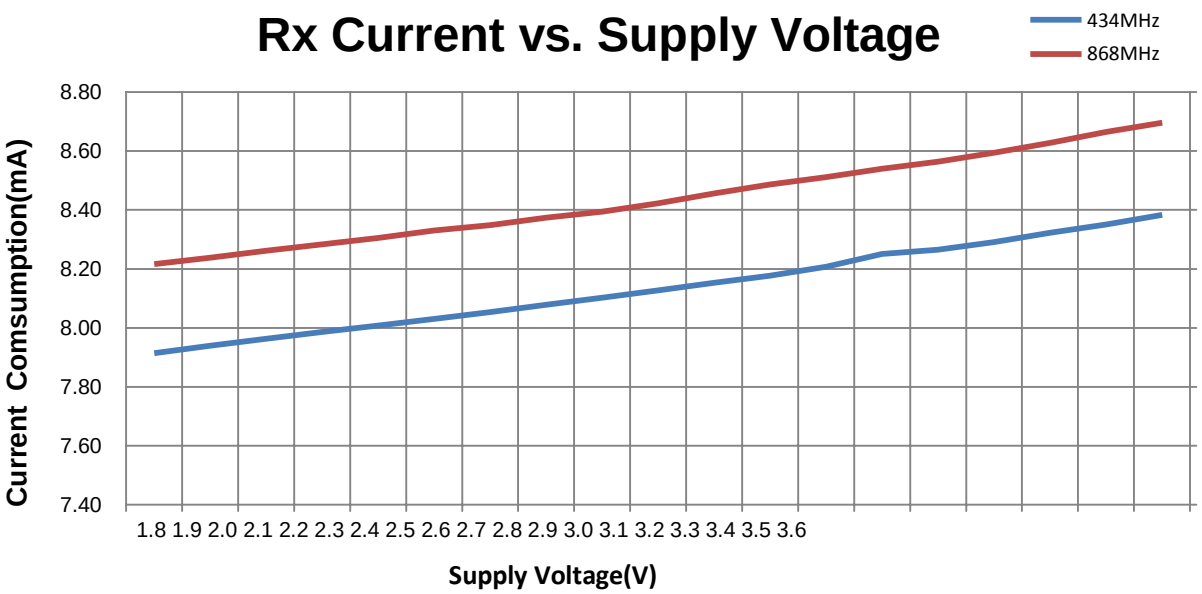
Table 8. Low Frequency Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Calibration frequency [1]	F_{LPOSC}			32		kHz
Frequency accuracy		After calibration		±1		%
Temperature coefficient [2]				-0.02		%/°C
Supply voltage coefficient [3]				+0.5		%/V
Initial calibration time	$t_{LPOSC-CAL}$			4		ms

Remarks:
[1]. The low frequency oscillator is automatically calibrated to the crystal oscillator frequency at the PUP stage and periodically calibrated at this stage.
[2]. After calibration, the frequency changes with temperature.
[3]. After calibration, the frequency changes with the change of the supply voltage.

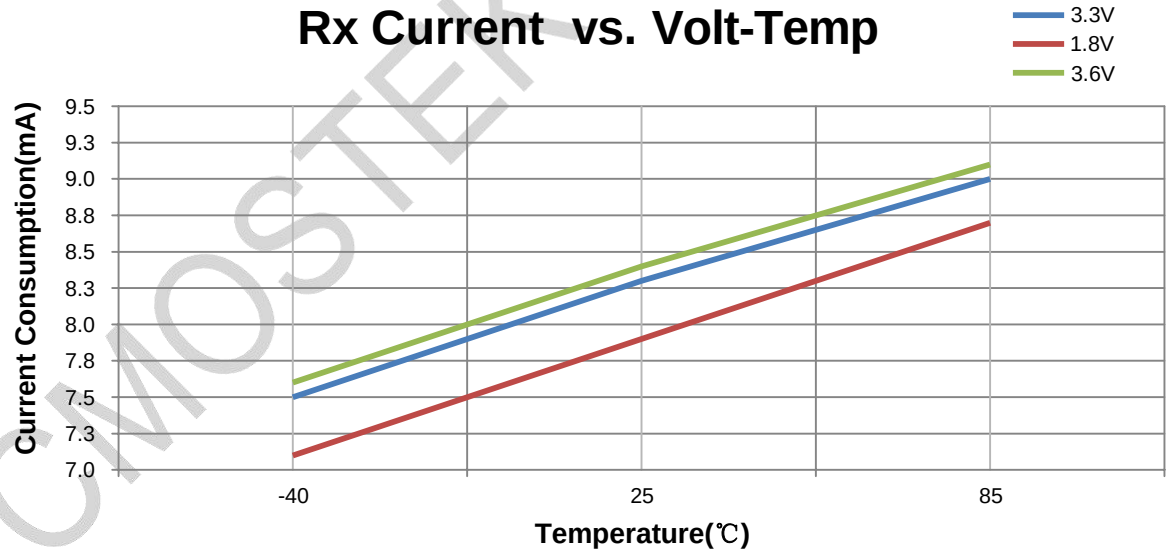
1.9 Figures of Critical Parameters

1.9.1 Rx Current VS. Supply Voltage

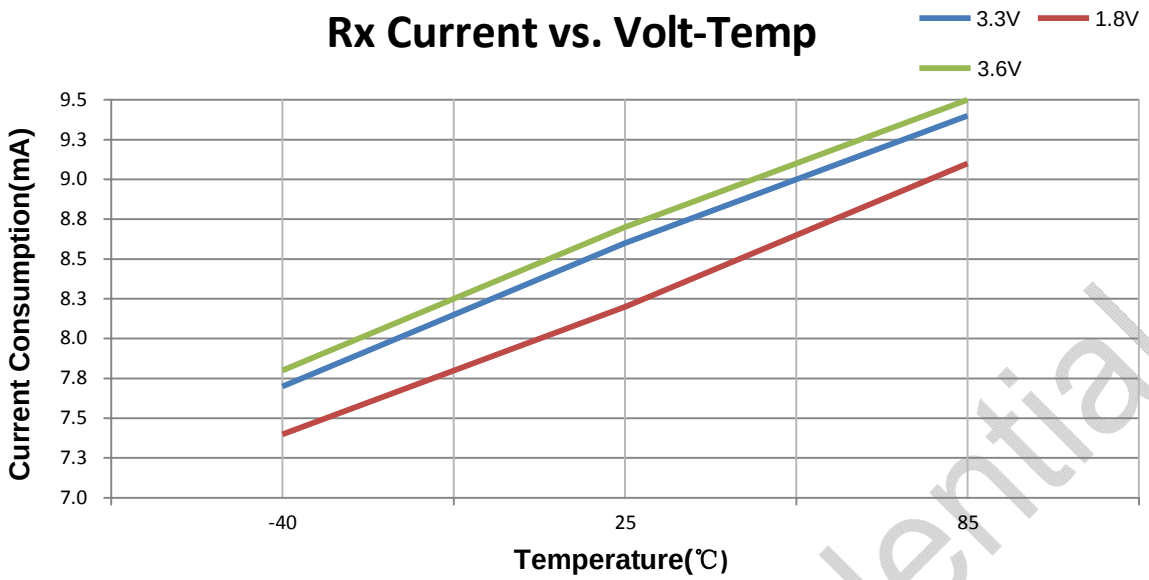


Testing Condition: Freq = 434MHz / 868MHz, Fdev = 10KHz, BR = 10Kbps

1.9.2 Rx Current VS. Voltage Temperature

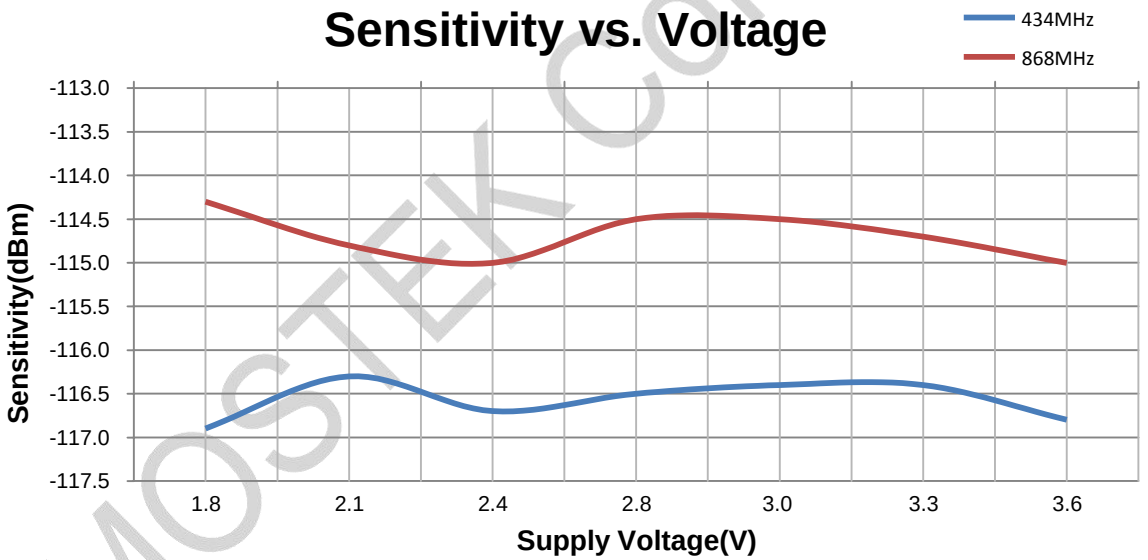


Test Condition: Freq = 434MHz,Fdev = 10KHz, BR = 10Kbps



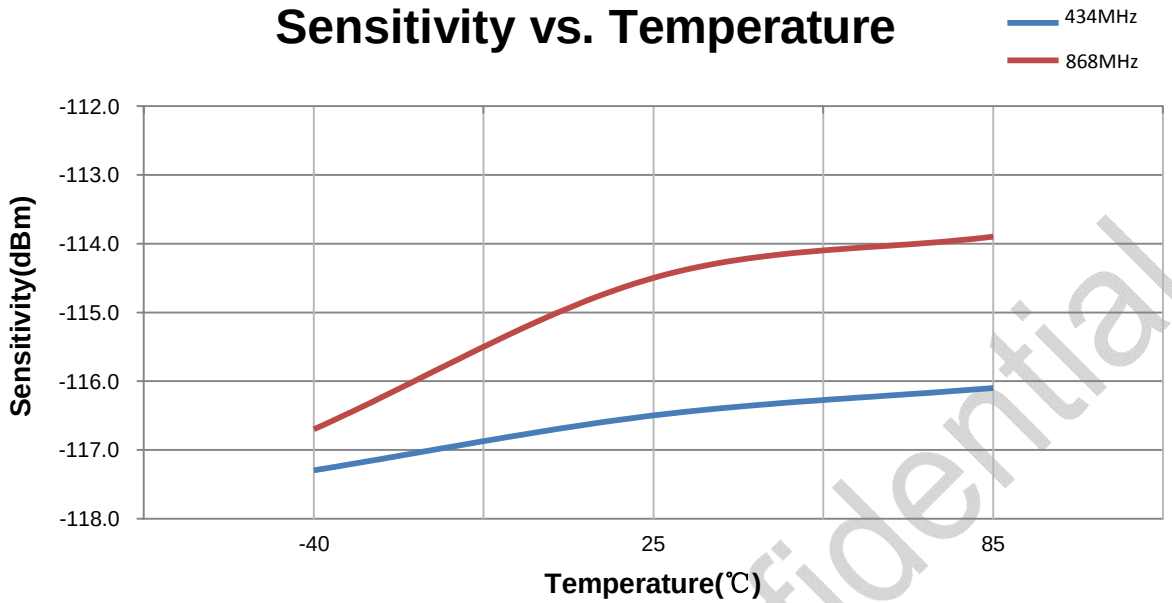
Test Condition: Freq = 868MHz, Fdev = 10KHz, BR = 10Kbps

1.9.3 Sensitivity VS. Voltage



Test Condition: FSK, DEV = 10KHz, BR = 10Kbps

1.9.4 Sensitivity VS. Temperature



Test Condition: FSK, DEV = 10KHz, BR = 10Kbps

2. Pin Descriptions

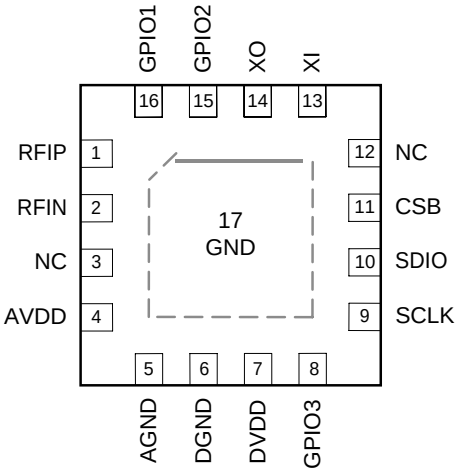
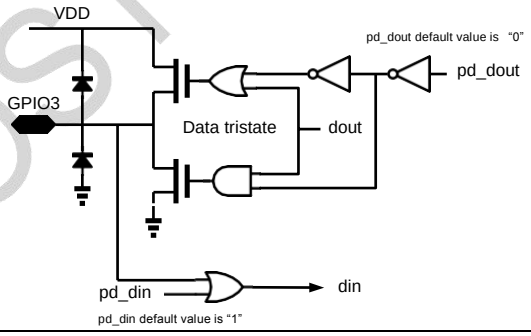
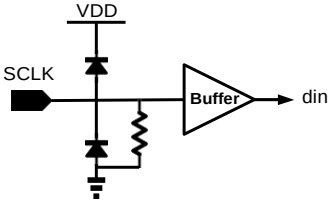
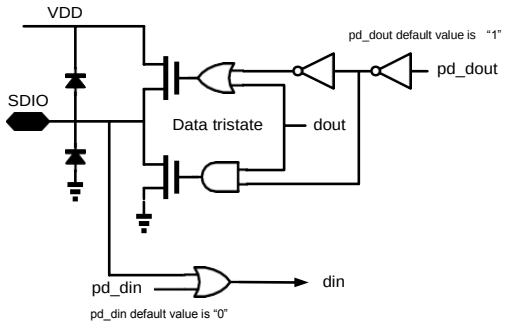
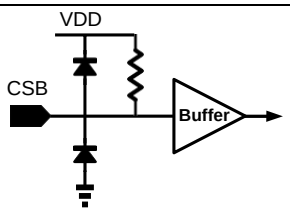
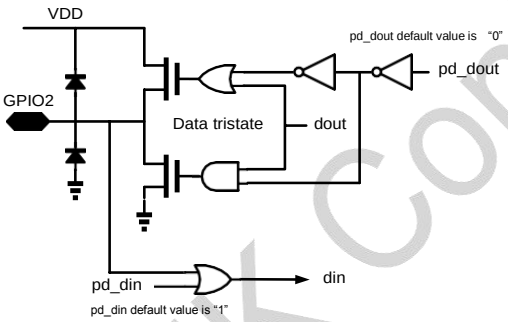
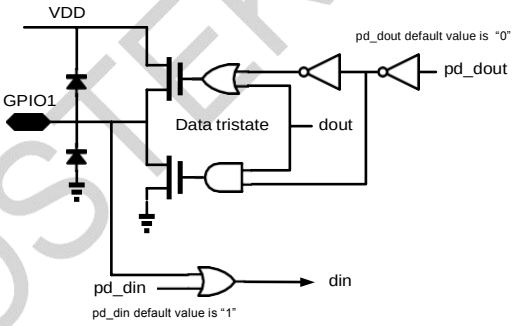


Figure 1. CMT2218B pin arrangements

Table 9. CMT2218B pin descriptions

Pin No.	Name	I/O	Internal IO Schematic	Descriptions
1	RFIP	I		RF signal input P
2	RFIN	I		RF signal input N
3	PA	O		Used, leave it floating
4	AVDD	IO		Analog VDD
5	AGND	IO		Analog GND
6	DGND	IO		Digital GND
7	DVDD	IO		Digital VDD
8[1]	GPIO3	IO		Configured as DOUT, RX_ACTIVE, DCLK
9	SCLK	I		SPI clock, internally with pull-down resistor. Only used for EEPROM burning.

10	SDIO	IO		SPI data input and output, internally with high impedance. Only used for EEPROM burning.
11	CSB	I		SPI chip selection bar for register access, internally with pull-up resistor. Only used for EEPROM burning.
12	NC	I		Used, leave it floating
13	XI	I		Crystal circuit input
14	XO	O		Crystal circuit output
15[1]	GPIO2	IO		Output RX_ACTIVE
16[1]	GPIO1	IO		OutputDOUT
17	GND	I		Analog GND. It must be grounded.

Note:

[1]. GPIO1, output DOUT: in Rx state, it outputs continues demodulated data; in other state, it outputs logic 0.

GPIO2, output RX_ACTIVE: it goes high at about 350 us before entering the Rx state, and goes low when exiting Rx state.

GPIO3, options: DOUT, RX_ACTIVE and DCLK. DCLK is the data rate clock synchronized to the demodulated data, used for the MCU to capture and decode the data.

[2]. SDIO has internal high impedance. User must add 10K pull-up resistor outside the chip to avoid possible leakage current.

3. Typical Application Schematic

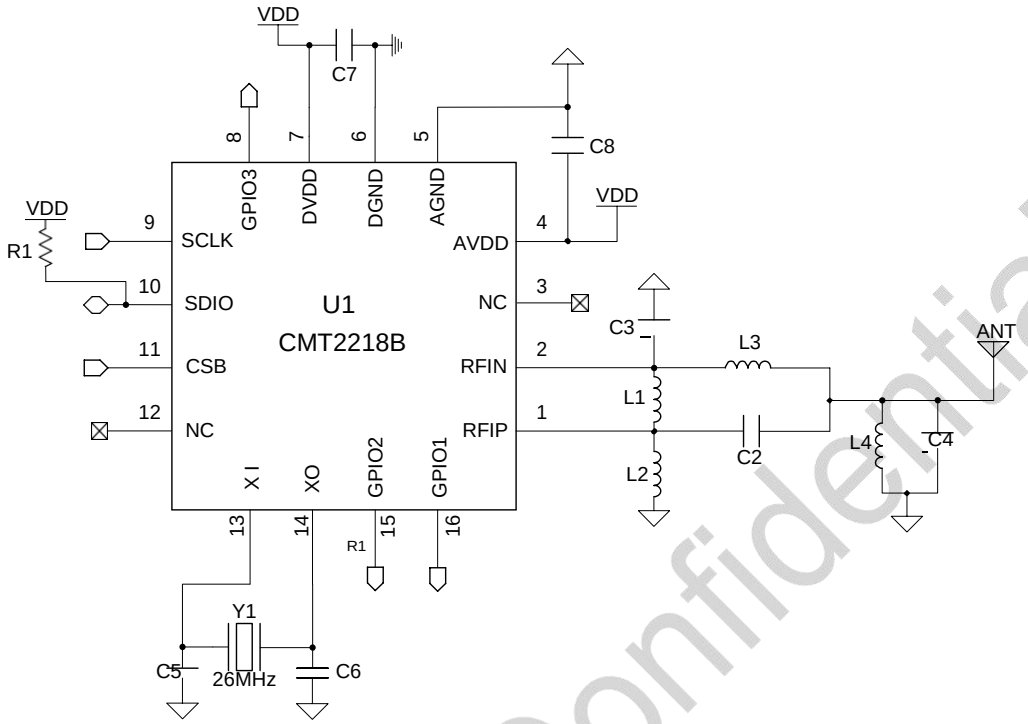


Figure 2. Application schematic diagram

Table 10. Application BOM

No.	Descriptions	Value			Unit	Supplier
		433 MHz	868 MHz	915 MHz		
R1	±5%, 0603,	10			KΩ	
C2	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C3	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C4	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C5	±5%, 0603 NP0, 50 V	24			pF	
C6	±5%, 0603 NP0, 50 V	24			pF	
C7	±5%, 0603 NP0, 50 V	470			pF	
C8	±5%, 0603 NP0, 50 V	0.1			uF	
L1	±5%, 0603 Multilayer chip inductor	68	12	12	nH	Sunlord SDCL
L2	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L3	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L4	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26			MHz	EPSON
U1	CMT2218B,Stand-Alone Sub-1GHzRF Receiver				-	CMOSTEK

4. Function Descriptions

CMT2218B is an ultra-low power, high performancereceiver chip. It uses a 26 MHz crystal oscillator as a reference clock for the internal PLL. It supports (G) FSK and (G) MSK, as well as stand-alone work mode without the need of being controlled by external MCU. It also supports various duty-cycle mode to reduce the current consumption and increase the stability. It is suitable for applications ranging from 140 to 1020MHz. The demodulated data is sent out directly from GPO. CMT2218B block diagramis as shown in the following figure.

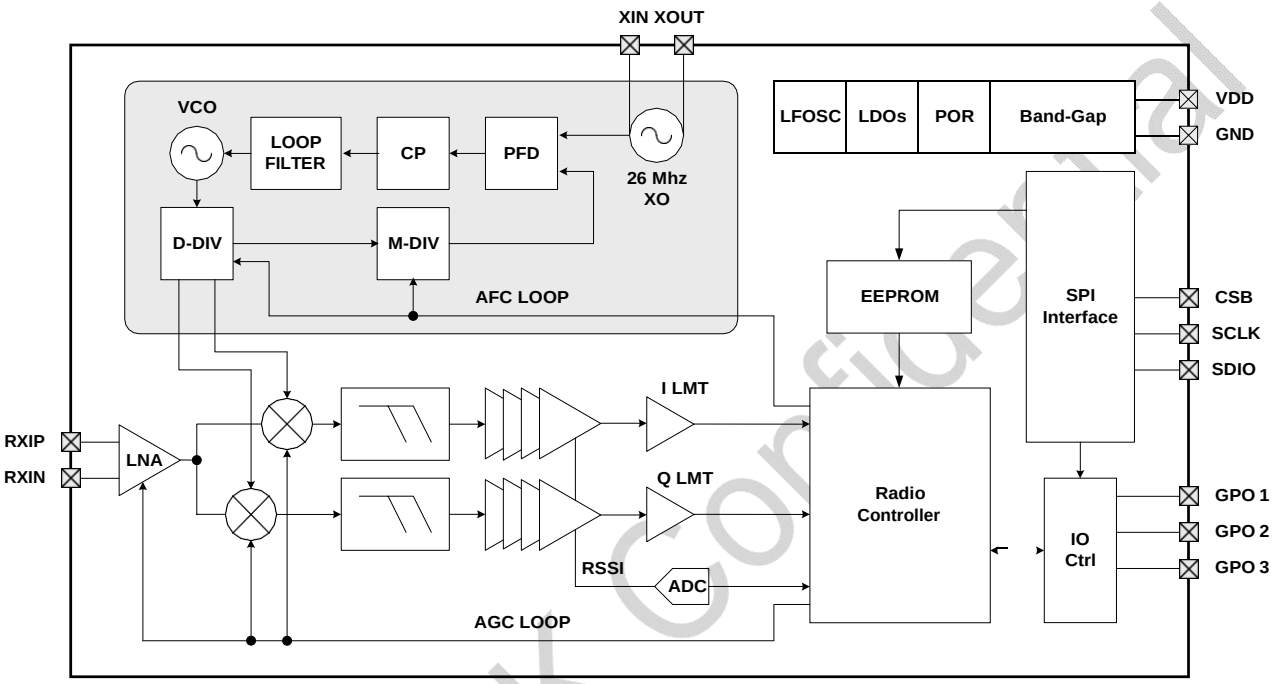


Figure 3. Functional Block Diagram

In the receiver part, the chip uses LNA+MIXER+IFFILTER+LIMITTER+PLL low-IF architecture to achieve the Sub-GHz wireless reception function.

In the receiver system, the analog circuit mixes the RF signal to IF and converts the signal from analog to digital through the Limiter module, then outputs I/Q two single bit signals to the digital circuit for (G) FSK demodulation. At the same time, SARADC will convert the real-time RSSI signal to 8-bit digital signal, and sent them to the digital part for the other processing. The digital circuit is responsible for mixing the intermediate frequency to zero frequency (Baseband) and performing a series of filtering and decision processing, while AFC and AGC control the analog circuit dynamically, finally the 1-bit original signal is demodulated and sent to the GPO directly.

The chip provides the SPI communication port for burning the EEPROM. Users need to use the tools provided by CMOSTEK.

4.1 Receiver

CMT2218B has a built-in ultra-low power, high performance low-IF FSK receiver. The RF signal induced by the antennais amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation. During power on reset (POR) each analog block is calibrated to the internal reference voltage. This allows the chip to remain its best performance at different temperatures and voltages. Baseband filtering and demodulation isdone by the digital demodulator.The AGC loop adjust the system gain by the broadband power detector and attenuation network nearby LNA, so as

to obtain the best system linearity, selectivity, sensitivity and other performance.

LeveragingCMOSTEK's low power design technology, the receiver consumes only a very low power when it is turned on. The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application with strict requirements of power consumption.

4.2 Auxiliary Blocks

4.2.1 Power-On Reset (POR)

The Power-On Reset circuit detect the change of the VDD power supply, and generate the reset signal for the entire CMT2218B system. After the POR, the MCU must go through the initialization process and re-configure the CMT2218B. There are two circumstances those will lead to the generation of POR.

The first case is a very short and sudden decrease of VDD. The POR triggering condition is, VDD dramatically decreases by 0.9V +/- 20% (e.g. 0.72V – 1.08V) within less than 2 us. To be noticed, it detects a decreasing amplitude of the VDD, not the absolute value of VDD.

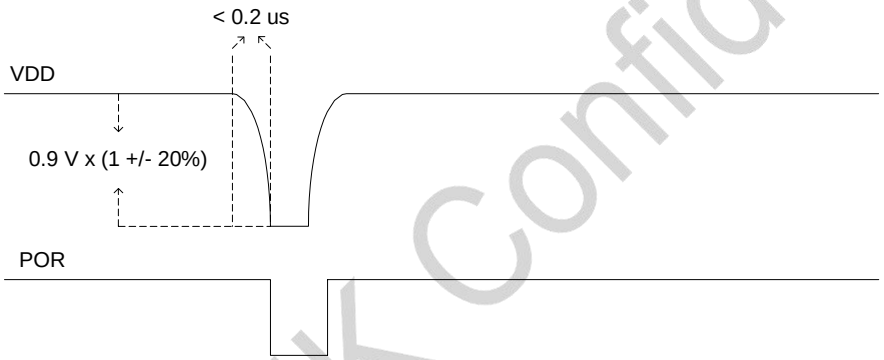


Figure 4. Sudden Decrease of VDD lead to Generation of POR

The second case is, a slow decrease of the VDD. The POR triggering condition is, VDD decreases to 1.45V +/- 20% (e.g. 1.16V – 1.74V) within a time more than or equal to 2 us. To be noticed, it detects an absolute value of VDD, not a decreasing amplitude.

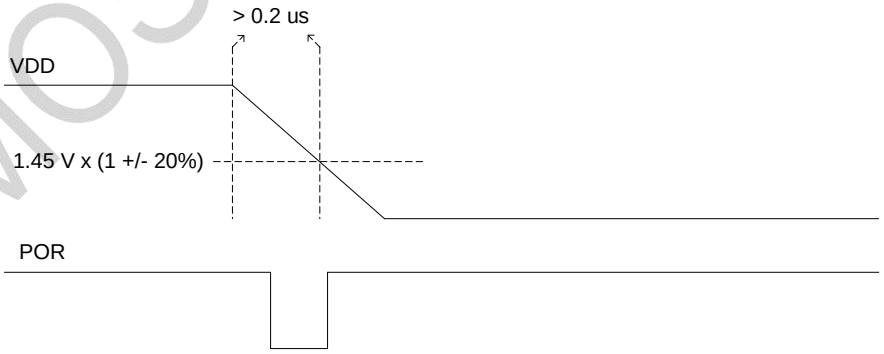


Figure 5. Slow Decrease of VDD lead to Generation of POR

4.2.2 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for the digital circuits. The value of load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL, in order to make the crystal accurately oscillate at 26 MHz.

C15 and C16 are the load capacitancesat both ends of the crystal. Cpar is the parasitic capacitance on the PCB. Each crystal pin has 5pF internal parasitic capacitance, together is equivalent to 2.5pF. The equivalent series resistance of the crystal must be within the specifications so that the crystal can have a reliable vibration. Also, an external signal source can be connected to the XI pin to replace the conventional crystal. The recommended peak value of this clock signal is from 300mV to 700mV. The clock is coupled to XI pin via a blocking capacitor.

4.2.3 Sleep Timer

The CMT2218B integrates a sleep timer driven by 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer wakes the chip from sleep periodically. When the chip operates in a duty cycle mode, the sleep time can be configured from 0.03125 ms to 41922560 ms. Due to the low power oscillator frequency will change with the temperature and voltage drift, it will be automatically calibrated during power on and will be periodically calibrated since then. These calibrations will keep the frequency tolerance of the oscillator within + 1%.

4.2.4 Received Signal Strength Indicator(RSSI)

RSSI is used to evaluate the signal strengthinside the channel. The cascaded I/Q logarithmic amplifier amplifies the signal before it is sent to the demodulator. The logarithmic amplifier of I channels and Q channel contains the received signal indicator, in which the DC voltage is generated is proportional to the input signal strength. The output of RSSI is the sum of thevalues of the two channels' signals. The output has 80dB dynamic range above the sensitivity. After the RSSI output is sampled by the ADC and filtered by a SAR FILTER and a RSSI AVG FILTER. The order of the average filter can be set by RSSI Filter Setting on RFPDK. The code value is translated into dBm value after filtering and compare with the RSSI_Compare_TH. If the RSSI is larger than the threshold it outputs logic 1, otherwise outputs logic 0. The output can be used as the receive time extending condition in the super low power (SLP) mode.

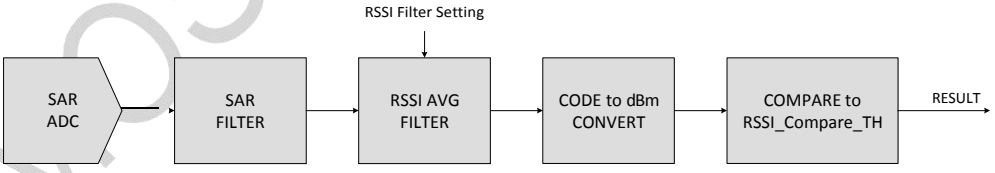


Figure 6. RSSI detection and comparison circuit

CMT2218B has done a certain degree of calibration before delivery. In order to obtain more accurate RSSI measurement results, the user needs to recalibrate the RSSI circuit in their dedicated applications. For further information, please refer to the "AN181-CMT2218BW RSSI Usage Guideline".

4.2.5 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in FSK demodulation, itcan automatically observe the phase jump characteristics of the received signal to determine whether it is awanted signal or an unwanted noise.

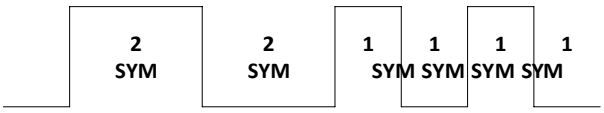


Figure 7. Received signal jump diagram

The PJD mechanism defines that the input signal switching from 0 to 1 or from 1 to 0 is a phase jump. Users can configure the PJD Window to determine the number of detected jumps for the PJD to identify a wanted signal.As shown in the above figure, in total 8 symbols are received. But the phase jump only appeared 6 times. Therefore, the number of jumpsis not equal to the number of symbols. Only when a preamble is received theyare equal.In general, the more jumps are used to identify the signal, the more reliable they result is; the less jumps are used, the faster the result is obtained.If the RX time is set to a relatively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps allow pretty reliable result, e.g. the chip will not mistakenly treat an incoming noise as a wanted signal, and vice versa will not treat a wanted signal as noise.

Detecting the phase jump of a signal, is identical to detect whether the signal has the expecteddata rate. In fact, at the same time, the PJD will also detect the FSK deviation and see if it is legal, as well as to see if the SNR is over 7 dB.With these three parameters the PJD is able to make a very reliable judgement. If the signal is wanted it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, or the receive time extending condition in the super low power (SLP) mode. In direct data mode, by enabling the Dout Mute, the PJD can mute the FSK demodulated data output while there is not wanted signal received.

The PJD technique is similar to the traditional carrier sense technique, but more reliable. While users combine the RSSI detection and PJD technique, they can precisely identify the status of the current channel.

4.2.6 Automatic Frequency Control (AFC)

The AFC mechanism allows the receiver to minimize the frequency error between the TX and RX in a very short time once a wanted signal comes in. This helps the receiver to maintain its highest sensitivity performance. CMT2218B has the most advanced AFC technology. Compare with the other competitors, within the same bandwidth, CMT2218B can identify larger frequency error, and remove the error in a much shorter time (8-10 symbols).

Normally the frequency error between the TX and RX is caused by the crystal oscillators used in both sides. CMT2218B allows the user to fill in the value of crystal tolerance (in PPM) on RFPDK. Based on the crystal tolerance, the RFPDK will calculate the AFC range whileminimizing the receiver bandwidth (to maintain the best performance). Due to the excellent performance of the AFC, it provides a good solution to the crystal aging problem which would lead to more frequency error as time goes by. Therefore, compare to other similar receiver chips, CMT2218B can solve more severe crystal aging problem and effectively extend the life time of the product.

4.2.7 Clock Data Recovery (CDR)

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate, while receiving the data. Not only for processing the data inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data.So CDR's task is simple and important. If the recovered clock frequency is in error with the actual symbol rate, it will cause data acquisition errors at the time of reception.

CMT2218BW has designed three types of CDR systems, as follows:

1. **COUNTING system**–The system is designed for the symbol rates to be more accurate. If the symbol rate is 100% aligned, the unlimited length of 0 can be received continuously without error.

2. **TRACING system** –The system is designed to correctthe symbol rate error. It has the tracking function. It can automatically detect the symbol rate transmitted by TX, and adjust quickly the local symbol rate of RX at the same time, so as to minimize the error between them.The system can withstand up to 15.6% or symbol rate error. Other similar products in the industry cannot reach this level.

3. **MANCHESTER system** –This system evolves from the COUNTING system. The basic feature is the same.The only difference is that the system is specially designed for Manchester codec.Special processing can be done when the TX symbol rate has unexpected changes.

5. ChipOperation

5.1 Operation State, Timing and Power Consumption

5.1.1 Startup Timing

After the chip VDD is powered up, the chip usually needs to wait about 1ms, then POR will release. After the release of the POR, the crystal will start, the start time is 200 us - 1 ms, depending on the characteristics of the crystal itself. After starting, the user need to wait for the crystal settled, then the system starts working. The default setting is 2.48ms. This time can be modified by writing XTAL Stable Time afterword (it has to be longer than the crystal inherent settling time). However, if the inherent settling time of the crystal is difficult to observed by the user, the default setting of 2.48 ms is recommended and is able to cover most of the crystals.

The chip remains in the IDLE status until the crystal is settled. After the crystal is settled, the chip will leave the IDLE state and begin to do the calibration of each module. After the calibration is completed, the chip will enter the duty-cycle working mode, or always stay in the Rx state until power down.

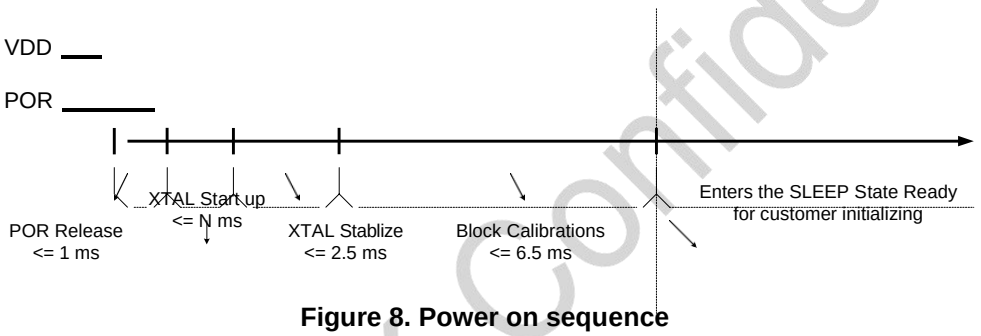


Figure 8. Power on sequence

5.1.2 OperationState

CMT2218B has 2operationstates: SLEEP and RX.

- **SLEEP State**

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.

- **RX State**

All modules on the receiver will be opened in RX state. Switching from SLEEP to RX needs to add the crystal start-up and settled time.

After the internal EEPROM of CMT2218B is successfully burned, the chip will enter the receive mode after power up. There are 2 receive modes available. One is the Always Receive Mode which turns off the duty-cycle operation. Another is the duty-cycle receive mode, which constantly switches the state between RX and SLEEP according to the user's configurations, as well as supports the Super Low Power (SLP) control mechanism.

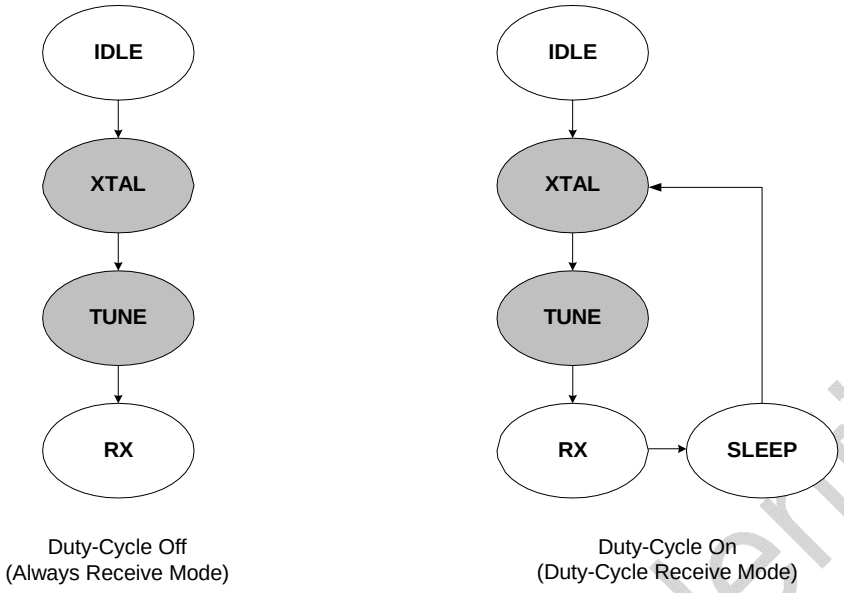


Figure 9. CMT2218B State Switch Diagram

The XTAL and TUNE in the figure are not specific states, but processes. XTAL stands for the process of crystal oscillator starting up and stabilizing.TUNE stands for the process of PLL locking and frequency tuning, taking about 350 us to complete. The RX and SLEEP time are configured on the RFPDK by the users. To be noticed, if the chip works in the duty-cycle receive mode, each time it wakes up from SLEEP, it will wait for the crystal oscillator to start up and get stable before entering the RX state.

6. Low Power Operation

6.1 Supper Low Power (SLP) Receive Mode

CMT2218B provides a set of options to help users achieve supper low power consumption (SLP - Supper Low Power) reception under different application requirements.These options can be used in the duty-cycle receive mode. The principle of the SLP mechanism is to shorten the Rx time when there is no wanted signal coming in, and properly extend the Rx time when there is wanted signal detected, so that the power consumption is minimized while the stability of reception is guaranteed.The traditional short-range wireless receiver generally uses the following basic scheme to achieve low powercommunication.CMT2218B is also compatible with this scheme, and expands it to2 more power-saving schemes. The figure below introduces the most basic scheme, which can be realized by the normal duty-cycle receive mode, as well as the two super-low-power schemes extended from the basic one.

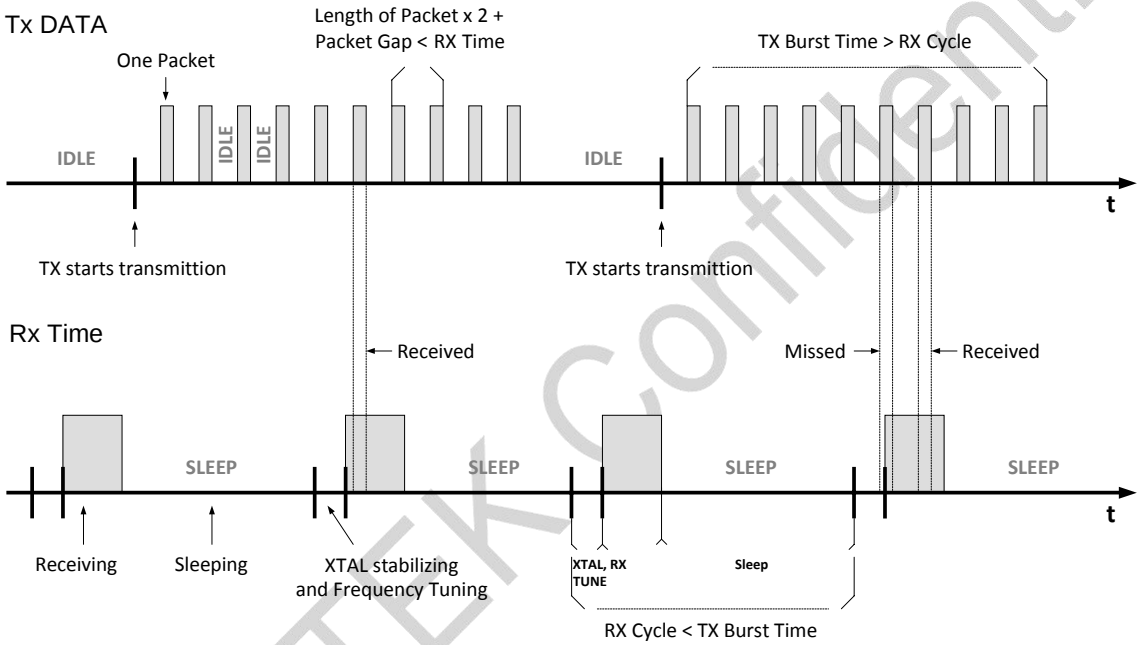


Figure 10. Basic low-power receiver scheme

Table 11. Low-power receiver mode

No.	Rx Extended Methods	Rx Extended Condition
4	Once detect RSSI_VLD = 1 during T1, leave T1 and stays in Rx state, exit Rx state until RSSI_VLD = 0.	RSSI_VLD is valid.
5	Once meet the Rx extended condition during T1, switch to T2. Exit Rx as soon as T2 timed out.	RSSI_VLD is valid

The T1 and T2 mentioned in the table refer to the RX T1 and the RX T2 time interval that can be set via the registers or RFPDK. The source of RSSI_VLD can be the comparison result of the RSSI or the detection result of the phase jump detector (PJD). For more details, please refer to “AN179-CMT2218BW Low Power Mode Usage Guideline”.

6.2 Receiver “Power VS Performance” Configuration

CMT2218B provides a set of registers to select the power consumption and sensitivity performance of the RF frontend circuit. The higher the performance is set, the higher the current is consumed.

7. RFPDK Configuration Interface

RFPDK is a Windows based software tool provided by CMOSTEK for configuring the RF products. For CMT2218B, the user can configure the chip by filling all the parameters on the interface, then burn the EEPROM inside the chip using the CMOSTEK programmer.

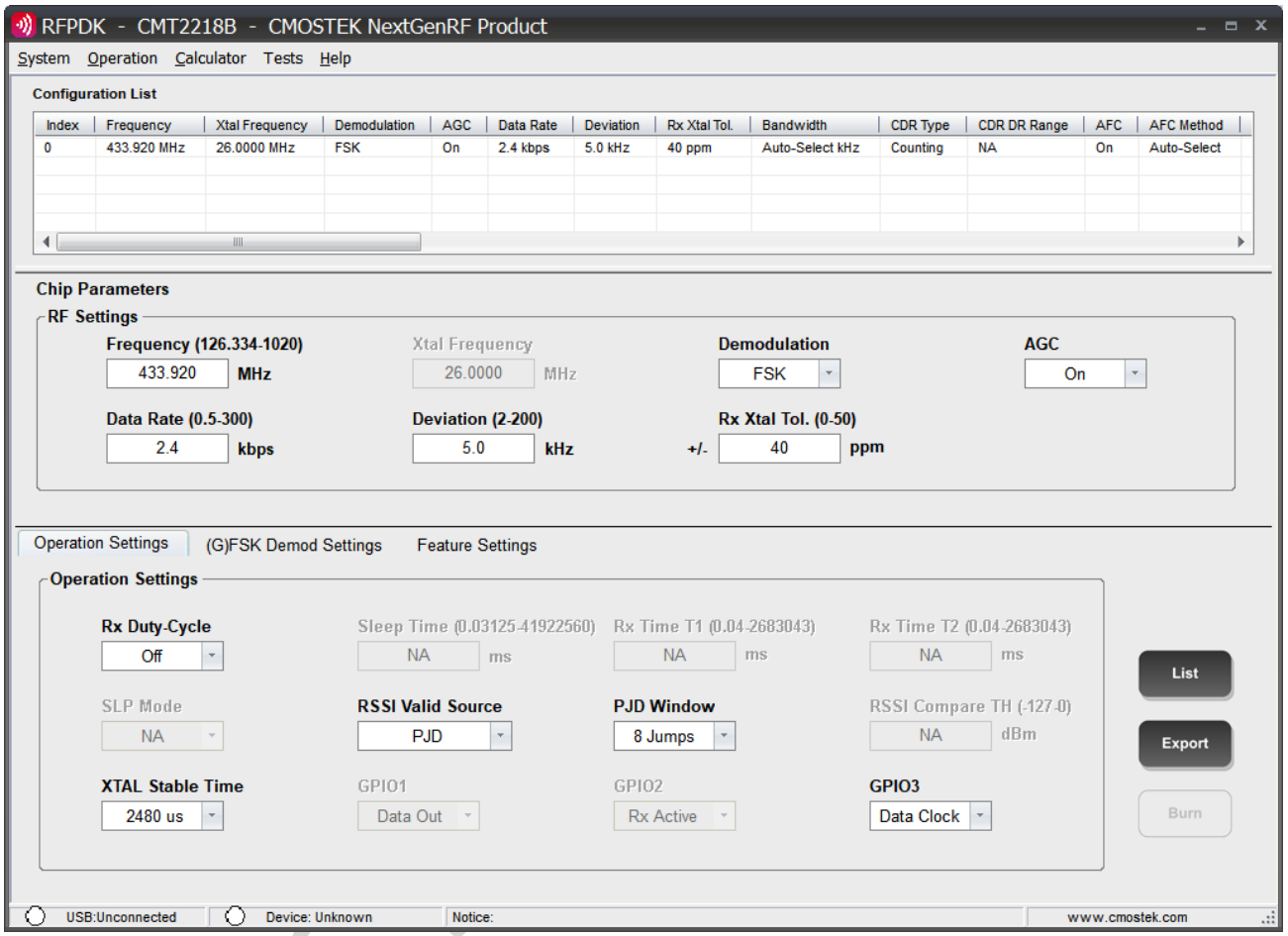


Figure 11. RFPDK configuration interface

8. Ordering Information

Table12. CMT2218B ordering information

Part Number	Descriptions	Packaging	Packing	Condition	MOQ
CMT2218B-EQR[1]	CMT2218B, Stand-Alone Sub-1GHz (G)FSK RF receiver	QFN16 (3x3)	Tape& Reel	1.8 to 3.6V, -40 to 85℃	3,000

Note:

[1]. "E" represents extended industrial grade.The temperature range is from -40 to +85.

"Q" represents QFN16 packaging.

"R" represents tape &reel packing. MOQ is 3000pcs.

For more information about product, please visitwww.cmostek.com.

For purchasing or price requirements, please contactsales@cmostek.com or local sales representative.

9. Packaging Information

CMT2218B packaging is QFN16 (3x3). The packaging information is as below.

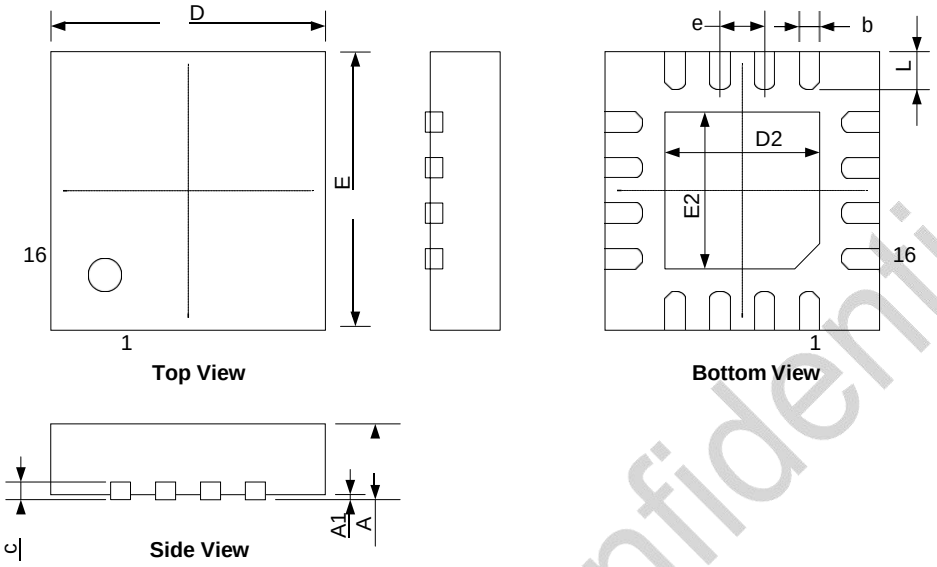


Figure12. 16-Pin QFN 3x3 packaging

Table13. 16-Pin QFN 3x3 Packaging Size

Symbol	Size (mm)	
	Min.	Max.
A	0.7	0.8
A1	—	0.05
b	0.18	0.30
c	0.18	0.25
D	2.90	3.10
D2	1.55	1.75
e	0.50 BSC	
E	2.90	3.10
E2	1.55	1.75
L	0.35	0.45

10. Top Marking

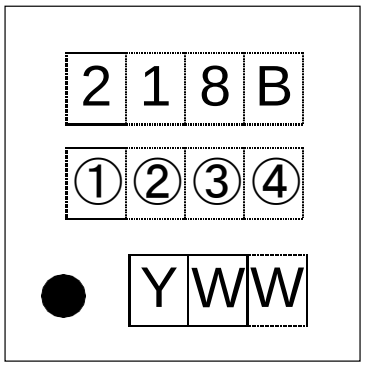


Figure 13. CMT2218B top marking

Table14. CMT2218B top marking description

Marking method	Laser
Pin 1 mark	Circle diameter = 0.3 mm
Font size	0.5 mm, right aligned.
Line 1 marking	218B represents model CMT2218B
Line 2 marking	①②③④ **represents th**e internal tracking coding
Line 3 marking	Date code is assigned by assembly factory. Y represents the last digit of the year. WW represents working week.

11. Document Change List

Table15. DocumentChange List

Rev. No.	Chapter	Change Descriptions	Date
Preliminary	All	Preliminary version for internal verification	2017-08-07
0.2	5	Change some descriptions	2017-08-15
0.3	All	Change some descriptions	2017-08-18
0.4	3	Added ROM list	2017-09-04
0.5	All	Full update	2018-01-08
0.6	4.2.6	Remove AN196 reference document	2020-09-11

12. Contact Information

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