



swarm bee V2 to V3 PCB Layout Migration

1.0

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1. Introduction

This application note describes the necessary PCB layout modifications to migrate an existing swarm bee LE V2 design to a new swarm bee LE V3 design. The swarm bee LE V3 module is smaller in size and has fewer pins than swarm bee LE V2. The order of the pins of the swarm bee LE V3 module have been assigned to maintain similarity to the swarm bee LE V2 module, and to make the migration of the layout as easy as possible.

The swarm bee LE V3 module is electrically equivalent to the swarm bee LE V2. Thus, no electrical adaptations, level shifting, etc. are necessary. The same applies to the API which is fully backwards compatible to the swarm bee LE V2 FW. To reduce the size of the module, the swarm bee LE V3 has castellated pads with a pitch of 1.6 mm in contrast to the swarm bee LE V2 having flat pads with a pitch of 2.0 mm.

This document compares the pinout of the two modules and depicts possible layout configurations. After reading this application note, the user should be able to modify the layout of their LE V2 PCB to accommodate the swarm bee LE V3.

For further details, refer to the swarm bee LE V3 data sheet [1] and the swarm API 3.0 User Guide [2] and for comparison the swarm bee LE V2 data sheet [3].

2. Mechanical differences

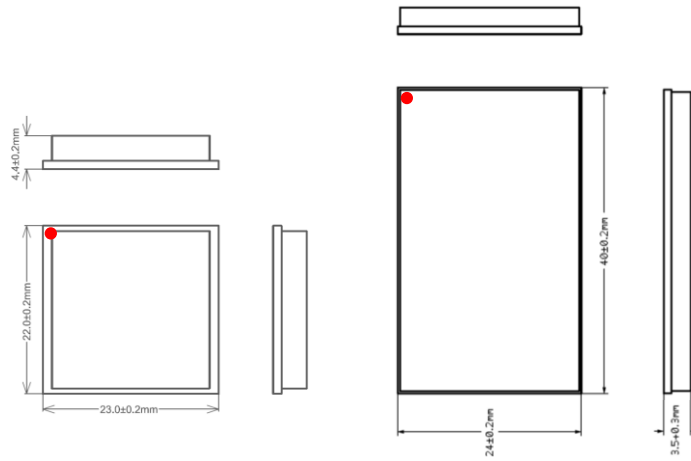


Figure 1 mechanical comparison

3. swarm bee LE V2 Pin Assignment

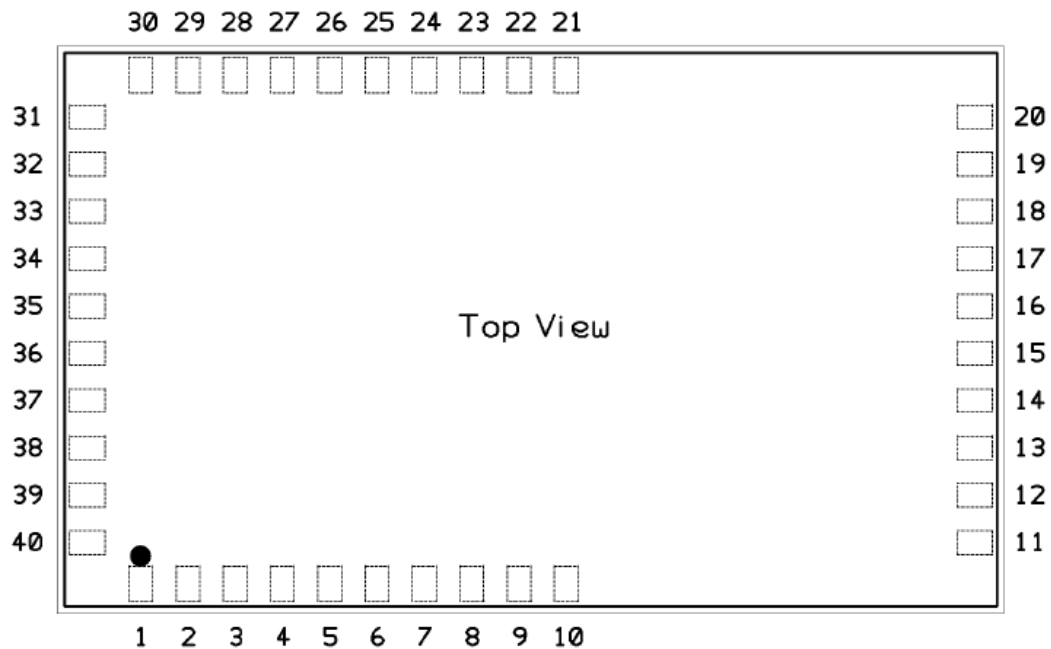


Figure 2 swarm bee LE V2 pin assignment, seen from top side

Table 1 swarm bee LE V2 pin assignment

Pin No.	Pin Name	Pin type*)	Pin Description	Electrical Conditions
1	Reserved			must be left open
2	VIN	Power	Power Supply	+ 3.0 V ... + 5.5 V, max. 120mA @3.3V
3	GND	Power	Circuit Ground	
4	A_MODE	I / FT	Autonomous Mode	- set the <i>swarm</i> bee LE into external controlled or autonomous mode - autonomous: high level (default setting via internal pull-up 45k resistor) - external controlled: external forced low level - buffered with a 1K series resistor
5	/NRST	I	Reset active low	optional
6	MOD_EN	I	disables <i>swarm</i> bee LE module	- module enabled: high voltage between +1.5 V and VIN (default setting via internal 5.6 M Ohm resistor) - module disabled: low voltage <0.4 V - buffered with a 1k series resistor
7	Reserved			must be left open
8	+2V6	O	2.6 V for level shifter	Max. 20 mA
9	Reserved			must be left open
10	GND			
11	/TX_RX	O	TX/RX indicator from nanoLOC	TX low, otherwise high. Buffered with a 1k series resistor. See also pin 35.
12	GND		RF Ground	
13	RF_PORT	RF	RF transmit and receive port	must be connected to a 50 Ohm termination
14	GND			
15	GND			
16	GND			
17	GND			
18	GND			
19	GND			

Pin No.	Pin Name	Pin type*)	Pin Description	Electrical Conditions
20	GND			
21	GND			
22	GND			
23	Reserved			must be left open
24	ADC_IN	I	Reads out the voltage relative to 2.6 V VDD	With an external voltage divider, the voltage can be read out. See [3] GBAT, SADC and GADC
25	DIO_0	I/O/FT	GPIO	buffered with a 1k series resistor
26	DIO_1	I/O/FT	GPIO	buffered with a 1k series resistor
27	DIO_2	I/O	GPIO	buffered with a 1k series resistor
28	Reserved			must be left open
29	UART_TX	O	serial interface transmit	buffered with a 1k series resistor
30	UART_RX	I / FT	serial interface receive	buffered with a 1k series resistor
31	Reserved			must be left open
32	Reserved			must be left open
33	Reserved			must be left open
34	DIO_3	I/O/FT	GPIO	buffered with a 1k series resistor
35	TX_ON	O	Transmission indicator (max.50 ms high after TX)	Max. pin current 25 mA, not more than 10 mA recommended buffered with a 120R series resistor. Recommended to be used with LED
36	DIV_COEX	O/FT	Can be used by external applications, see [4]	
37	Reserved			must be left open
38	Reserved			must be left open
39	Reserved			must be left open
40	Reserved			must be left open

***) Note:**

Pin type:

Power -> Power Supply
I -> Input
O -> Output
RF -> RF-Port
FT -> 5 V tolerant, max. input voltage 5.5 V

All logic levels except for 5 V tolerant inputs refer to 2.6 V VDD of the internal microcontroller

V_{OH} min 2.15 V
V_{OL} max 0.45 V
V_{IL} max 0.7 V
V_{IH} max 2.9 V (except 5 V tolerant inputs)

4. swarm bee LE V3 Pin Assignment

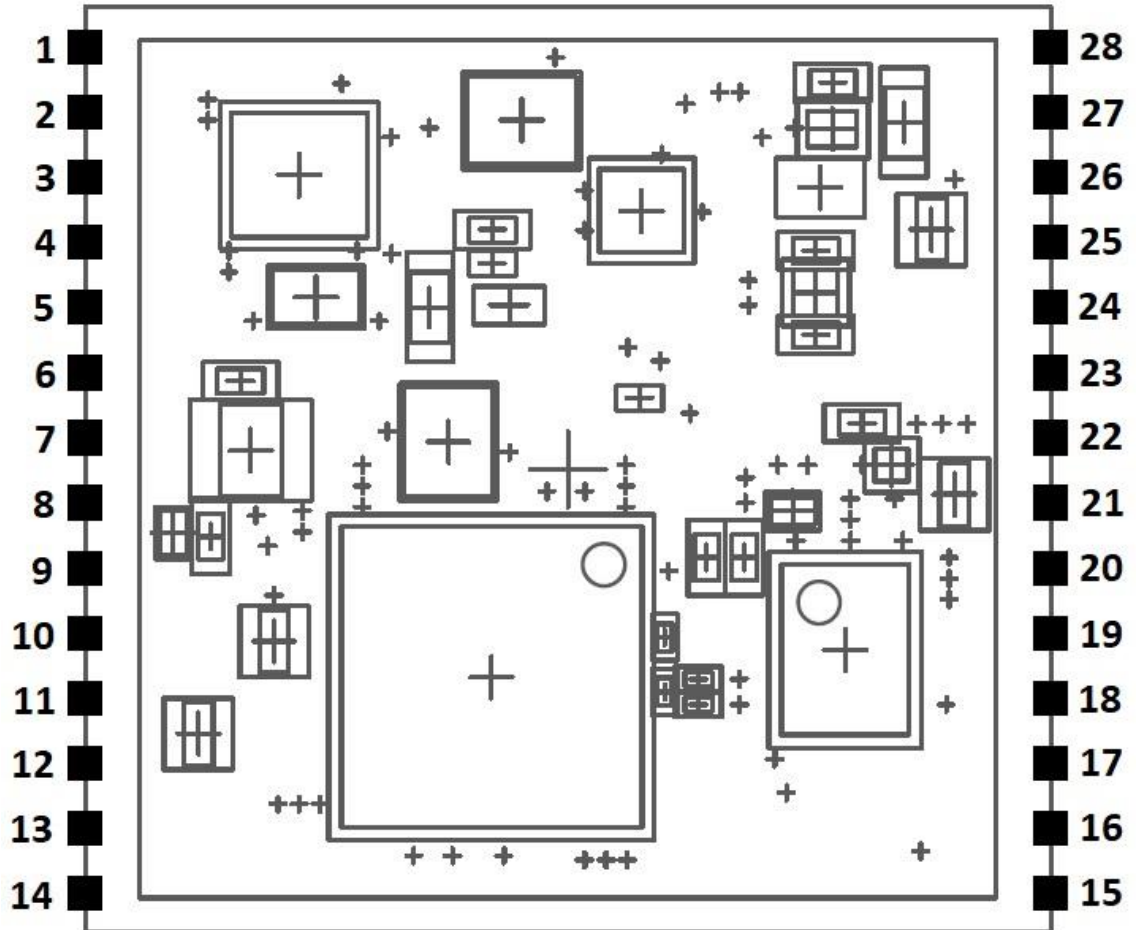


Figure 3 swarm bee LE V3 pin assignment, seen from top side

Table 2 swarm bee LE V3 pin assignment

Pin No.	Pin Name	Pin Type	Pin Description	Electrical Conditions
1	Reserved			must be left open
2	Reserved			must be left open
3	GND	Power	Circuit RF Ground	
4	Reserved			must be left open
5	GND	Power	Circuit RF Ground	
6	Reserved			must be left open
7	VIN	Power	Power Supply	+3.3V...+5.5V
8	GND	Power	Circuit Ground	
9	A_MODE	I/FT	Autonomous Mode	<ul style="list-style-type: none"> - set the <i>swarm bee LE V3</i> into external controlled or autonomous mode; - autonomous: high level (default setting via internal pull-up 13 kOhm resistor); - external controlled: external forced low level; - buffered with a 1 kOhm series resistor
10	/NRST	I	Reset active low	optional
11	MOD_EN	I	Disables swarm bee LE module	<ul style="list-style-type: none"> - module enabled: high voltage between +1.5 V and VIN (default setting via internal 5.6 MOhm resistor); - module disabled: low voltage <0.4 V; - buffered with a 1 kOhm series resistor
12	USART_TX	O	Serial interface transmit	buffered with a 1 kOhm series resistor
13	+2V6	O	2.6 V for external level shifter	max. 20 mA

Pin No.	Pin Name	Pin Type	Pin Description	Electrical Conditions
14	Reserved			must be left open
15	/TX_RX	O	TX/RX indicator from nanoLOC	- TX low, otherwise high; - buffered with a 1 kOhm series resistor.
16	GND	Power	Circuit RF Ground	
17	RF_PORT	RF	RF transmit and receive port	must be connected to a 50 Ohm termination
18	GND	Power	Circuit RF Ground	
19	USART_RX	I/FT	Serial interface receive	buffered with a 1 kOhm series resistor
20	GND	Power	Circuit Ground	
21	ADC_IN	I	Reads out the voltage relative to 2.6 V VDD	with an external voltage divider, the voltage can be read out
22	DIO_0	I/O/FT	GPIO	buffered with a 1 kOhm series resistor
23	DIO_1	I/O/FT	GPIO	buffered with a 1 kOhm series resistor
24	DIO_2	I/O	GPIO	buffered with a 1 kOhm series resistor
25	DIO_3	I/O/FT	GPIO	buffered with a 1 kOhm series resistor
26	TX_ON	O	Transmission indicator (max. 50 ms high after TX)	- max. pin current 25 mA, not more than 10 mA recommended buffered with a 120R series resistor; - recommended to be used with LED
27	DIV_COEX	O/FT	Can be used by external applications	
28	Reserved			must be left open

***) Note:**

Pin type:

Power -> Power Supply

I -> Input

O -> Output

RF -> RF-Port

FT -> 5 V tolerant, max. input voltage 5.5 V

All logic levels except for 5 V tolerant inputs refer to 2.6 V VDD of the internal microcontroller

V_{OH} min 2.15 V

V_{OL} max 0.45 V

V_{IL} max 0.7 V

V_{IH} max 2.9 V (except 5 V tolerant inputs)

5. swarm bee LE V2 to swarm bee LE V3 layout migration guideline

As shown in Table 3 and Figure 4, the pin order of the swarm bee LE V3, in the most cases, follows with an offset, the pin order of the swarm bee LE V2. This is why the modification of the board layout to replace the swarm bee LE V2 by the swarm bee LE V3 should be relatively straightforward. There are two options to modify the layout. The first is to leave the position of the RF port and re-route the signal lines- see section 5.1. The second is to align most of the signal lines and move the RF port- see section 5.2.

Table 3 swarm bee LE V3 vs swarm bee LE V2 Pin Assignment

Pin Name	swarm bee LE V3 PIN	swarm bee LE V2 PIN
Reserved	1	x
Reserved	2	x
GND	3	x
Reserved	4	x
GND	5	x
Reserved	6	1
VIN	7	2
GND	8	3
A_MODE	9	4
/NRST	10	5
MOD_EN	11	6
USART_TX	12	29
+2V6	13	8
Reserved	14	9
TX_RX	15	11
GND	16	12
RF_PORT	17	13
GND	18	14
USART_RX	19	30
GND	20	22
ADC_IN	21	24
DIO_0	22	25
DIO_1	23	26
DIO_2	24	27
DIO_3	25	34
TX_ON	26	35
DIV_COEX	27	36
Reserved	28	x

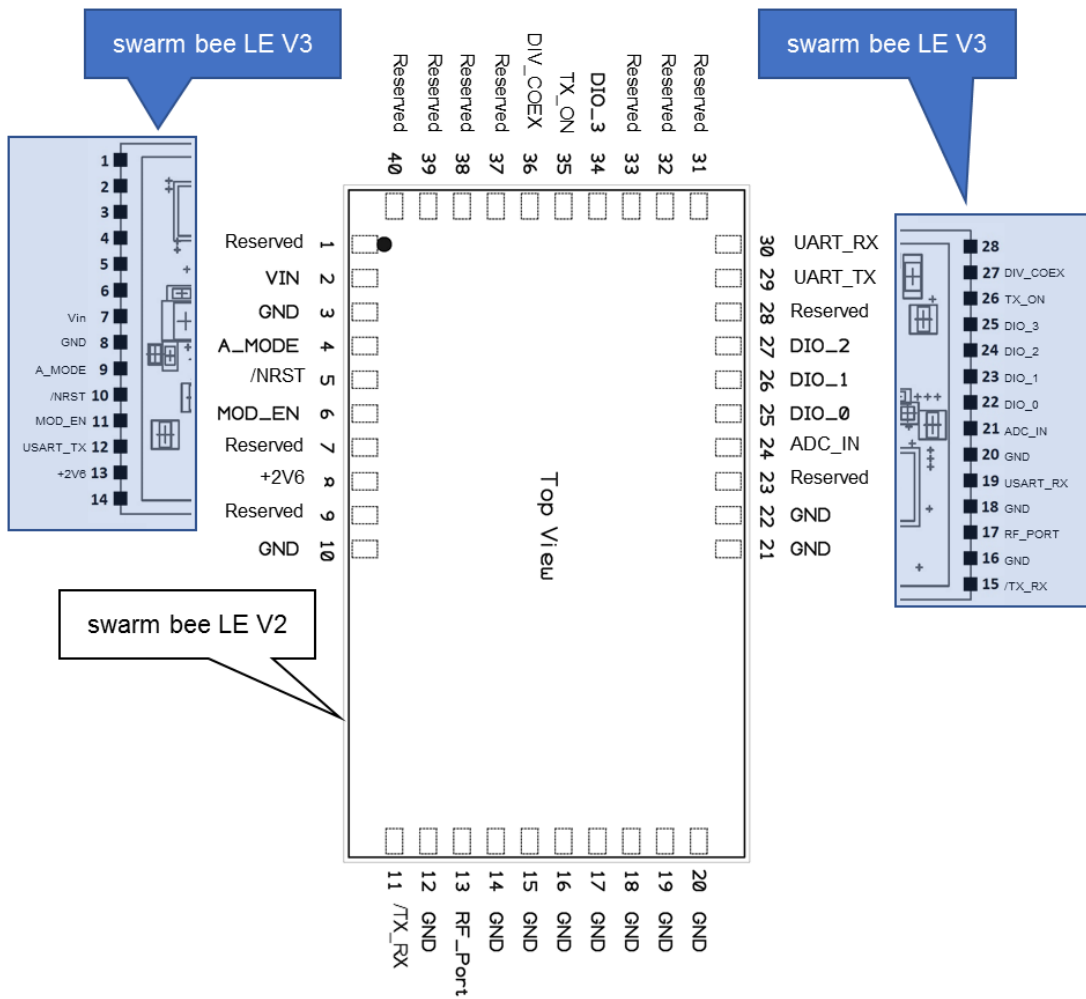


Figure 4 swarm bee LE V2- V3 pin assignment comparison

5.1. RF port as Reference

To begin, orient the swarm bee LE V3 on the board so that the RF port (the most critical pin) remains in the same place as the RF port on your swarm bee LE V2 layout, shown in Figure 5. Refer to Figure 2 and Figure 3 to identify the RF ports respectively. The RF port on the swarm bee LE V2 is pin number 13 and on the swarm bee LE V3 it is pin number 17. Thus, the edge of the swarm bee LE V3 module with pins 15 to 28 should be oriented in parallel to the top edge of the board (where a fictive SMA connector is mounted – see Figure 5). Please, note that pin 15 (TX_RX) on the V3 module is also two pins away from the TX_RX (pin 11) as on the V2 module (what also helps). After this step everything is ready to continue with the routing of the rest of the tracks which carry the digital signals and the power supply. The digital signals are not too demanding to route and can be routed as narrow traces running next to each other. *Important is to keep those (digital) lines away from the RF and the power supply lines to avoid noise coupling onto those analog lines.* An example how to isolate the lines is given in Figure 7. The pinout of the digital lines on swarm bee LE V3 essentially follows the pinout of the swarm bee LE V2 making the migration of the design easier. Regarding the power supply line Vin, it should be as thick as possible to avoid dynamic voltage fluctuations.

Note: No tracks should be routed directly underneath the bottom of the module, as it may cause lines to short and even destroy the module.

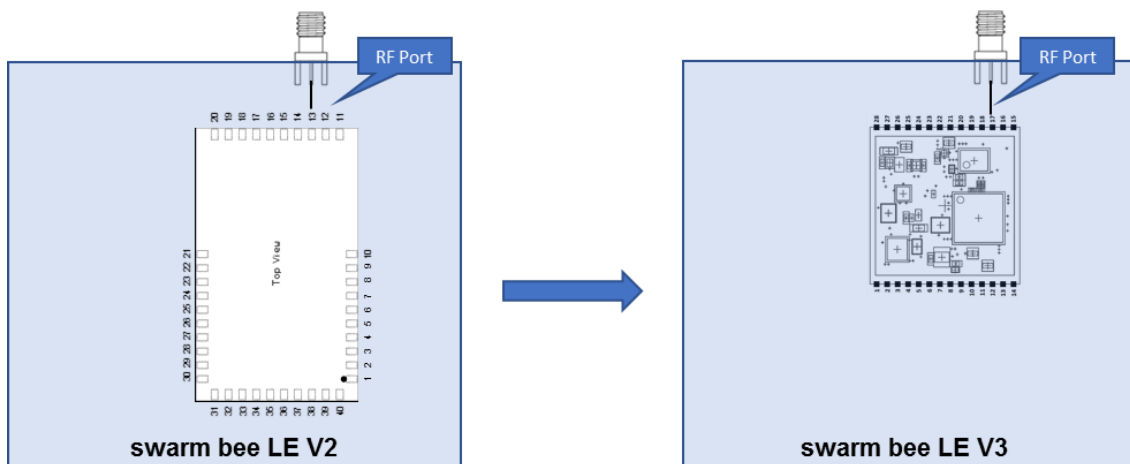


Figure 5 swarm bee LE V2 to V3 layout transition - RF port as reference

5.2. Digital Lines as Reference

The second option to modify the layout is to take the digital lines as reference which necessitates to move the layout of the RF port to the antenna or to re-route it. Latter can become critical. Looking at Figure 4 we have on one side the same order from pin Vin to +2V6 (except USART_TX), while on the other we have the same order from DIO_2 to ADC_IN. In this case the pads and lines can be narrowed to fit to the footprint of the swarm bee LE V3. The other lines must be re-routed. The position of the modules in contrast to each other is shown in Figure 6. As explained in the previous section, *it is important to keep the digital lines away from the RF and the power supply lines to avoid noise coupling onto those analog lines*. An example how to isolate the lines is given in Figure 7. Regarding the power supply line Vin, it should be as thick as possible to avoid dynamic voltage fluctuations.

Note: No tracks should be routed directly underneath the bottom of the module, as it may cause lines to short and even destroy the module.

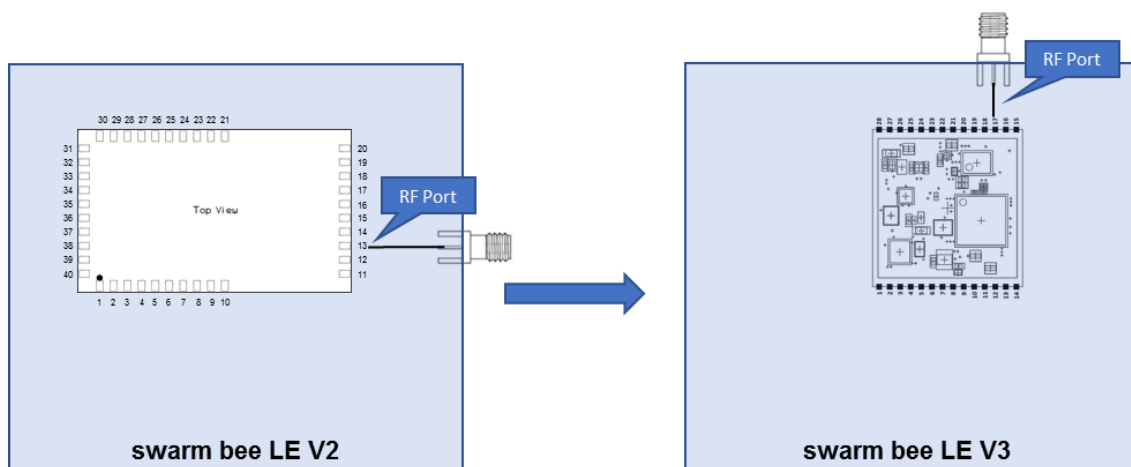


Figure 6 swarm bee LE V2 to V3 layout transition – digital lines as reference

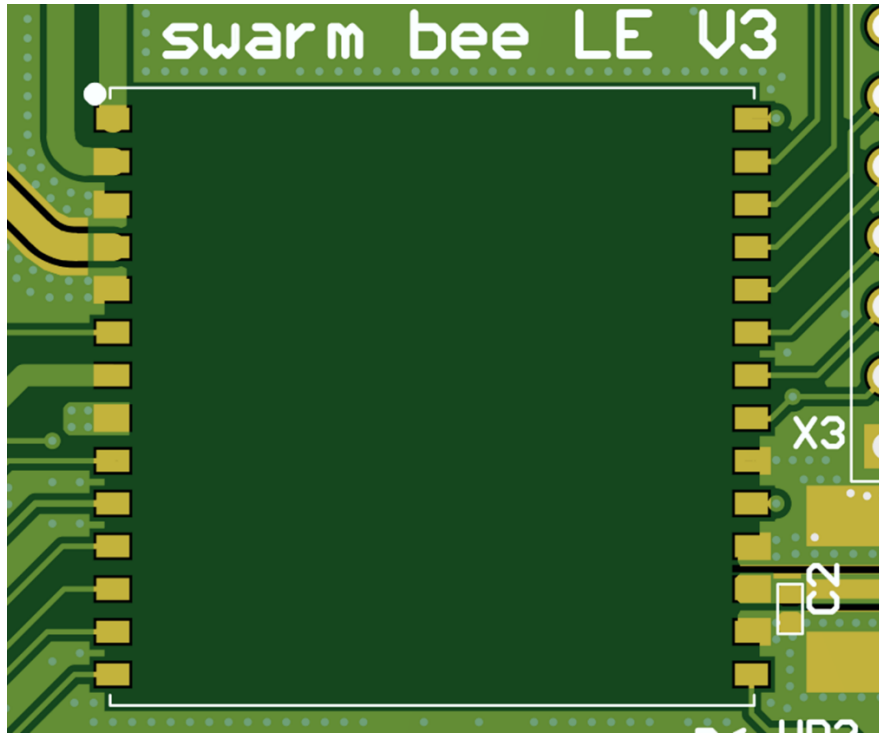


Figure 7 Layout example with ground isolation and vias

6. Conclusion

As it was shown in this application note, the swarm bee LE V3, although not fully 100% pin compatible with swarm bee LE V2 (due to reduced number of pins and smaller size), closely follows the pin order of the swarm bee LE V2. Therefore, the layout modification effort, in order to migrate from the swarm bee LE V2 to the swarm bee LE V3, is relatively low.

For additional details, refer to the swarm bee LE V3 data sheet [1] and the swarm bee LE V2 Data Sheet [3].

7. References

- [1] swarm bee LE V3 Data Sheet. Doc. Id. NA-19-0382-0024
- [2] swarm API 3.0 Doc. Id. NA-13-0267-0003
- [3] swarm bee LE V2 Data Sheet. Doc. Id. NA-16-0364-0042

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