ETRX35x-LRS and ETRX35xHR-LRS ZigBee® MODULES

Application Note –
Writing customised firmware for the ETRX35x-LRS

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1 Introduction

The ETRX357-LRS / ETRX357HR-LRS and ETRX351-LRS / ETRX351HR-LRS modules contain an Ember EM357 or EM351 ZigBee chip respectively, and a SiGe SE2432L front-end module with a low-noise receiver amplifier and an RF power amplifier. When using the Ember Insight tools to develop customised firmware for these modules, it is necessary to know how the EM35x controls the SE2432L since this information is specific to the Telegesis devices. This document gives details of the settings of various configuration registers in the EM35x that are necessary for correct operation.

Consult the ETRX35x-LRS Product Manual for details of the hardware platform, such as the pin-out, dimensions and electrical parameters.

2 Customising for the SE2432L

2.1 Control signal connections

Two signal lines from the EM35x that are brought out to ETRX35x pads are not available for external use in the ETRX35x-LRS as they are connected internally to the SE2432L chip. PC5 should not be connected to an external circuit in case it affects the switching performance of the SE2432L; PB0 from the EM35x chip is not connected to the ETRX35x-LRS pad at all.

ETRX35x-LRS			**SE2432L**	
Pad	Pin name	Other functions	Pin name	Function
25	PB0	VREF, IRQA	CSD	Chip select (power down)
			CPS	RX bypass
2	PC5	TX_ACTIVE	CTX	RX/TX mode

On the ETRX357-LR (which uses different RF components) PC5 is not available as this is configured as TX_ACTIVE. On the ETRX35x-LRS PB0 is not available either. Pads 2 and 25 are therefore designated “no connection”. The function of PB0 is to put the SE2432L into a low power state more quickly than is achieved by merely allowing its Vdd supply to decay when the EM35x is powered down, which reduces the average power consumption.

2.2 Firmware configuration

2.2.1 Configuring PC5

PC5 connected to the CTX pin of the SE2432L must be configured:

- either as the alternate output function TX_ACTIVE in register GPIO_PCCFGH
- or defining ENABLE_ALT_FUNCTION_TX_ACTIVE in the board header.

It will then be driven by the EM35x as required.

2.2.2 Configuring PB0

The CSD and CPS pins are both connected to PB0. Ember's EZSP or NCP firmware will automatically drive PB0 to power the unit up and down as required, but when writing custom firmware PB0 needs to be controlled at the application level. When writing custom firmware it is necessary to configure PB0 as an output and drive it low before going to sleep and high when waking up. This is best achieved by incorporating it into the halPowerDownBoard() and halPowerUpBoard() definitions in the board header file.

- PB0 needs to be set as an output in register GPIO_PBCFGL
- PB0 needs to be set in halInternalPowerUpBoard() (or at a different location)
- PB0 needs to be cleared in halInternalPowerDownBoard (or at a different location)

2.2.3 Automatic configuration

You can write firmware that is common to both the ETRX35x and the ETRX35x-LRS and read the manufacturing tokens to distinguish between the two devices. In the ETRX35x bit 1 of token TOKEN_MFG_PHY_CONFIG is set to 1, in the ETRX35x-LRS it is cleared to 0.

The Ember stack will read this token and automatically switch the RF output port to its alternate configuration, so that it uses separate input and output pins instead of a single bidirectional connection. However, if the user's firmware controls the RF port it must include the statement

```
emberSetTxPowerMode(EMBER_TX_POWER_MODE_ALTERNATE);
```

2.2.4 RF power level

Please also note that the gain of the SE2432L is quite high and therefore the output power of the EM35x needs to be reduced to the levels stated in section 11.2 of the ETRX35x-LRS manual to prevent driving the PA into saturation, which would result in non-compliant harmonic emissions.

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6 References

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